



# 2027 INTERNATIONAL TEST CONFERENCE

OCTOBER 10 - 15, 2027

Grand Hyatt San Antonio Riverwalk, TX, USA

## Call for Papers

Test is evolving faster than at any point in recent memory. AI workloads are driving large, power-hungry products built from chiplets, 3D stacks, high-bandwidth memory, and optical links, and each of these technologies raises new questions about how devices are screened, diagnosed, and trusted in the field. At the same time, AI is entering the test engineer's own toolbox, from pattern generation and data analytics to agent-assisted debugging. The International Test Conference (ITC), the premier forum for the electronic test of devices, boards, and systems across the full product lifecycle, invites you to help shape these emerging directions.

We seek original, unpublished papers on testing and testable design, whether they advance fundamental research or report hands-on industrial experience. Contributions on the topics listed at right, as well as on our specialized tracks, are especially welcome. Last year, we introduced the Large AI Systems & Shared Silicon Challenges and AI for Test Efficiency & Innovation tracks. **This year, we are particularly excited to introduce a new track:**

**Track: Co-Packaged Optics & Optical I/O.** As optical engines move into the package alongside the ASIC, test must address the electrical and optical domains together. We seek work on photonic IC test, known-good optical dies, wafer-level photonic probing, fiber-attach yield, optical link and loopback testing, and electro-optical co-debug methodologies.

### Submissions must include:

- Title of paper.
- Name, affiliation, e-mail address of each author.
- The corresponding author(s). ITC will communicate with the corresponding author(s).
- One or two topic(s) from the topic list, or a description of your topic.
- An electronic copy of a complete paper of up to 10 pages and an abstract of 100 words or less to be entered online.

**Important Note:** ITC maintains a competitive selection process. Submissions must clearly describe the work's status, contribution, novelty, and significance. Papers under simultaneous review or already accepted by another conference will be summarily rejected. Submissions shorter than 4 pages are rarely accepted. For AI-focused papers, an appendix of up to 6 pages may be submitted in addition to the main paper.

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|----------------------------------|----------------------|
| <b>Paper title/abstract due:</b> | <b>March 5, 2027</b> |
| <b>Paper final PDF due:</b>      | <b>April 9, 2027</b> |
| <b>Author notification:</b>      | <b>June 1, 2027</b>  |

We also welcome two-page poster proposals for late-breaking results, innovative methods seeking feedback, or participation without a full paper. Poster acceptance does not prevent future submission as an ITC paper in 2028. More information on posters will be provided on the ITC webpage.

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| <b>Poster submission deadline:</b> | <b>July 9, 2027</b>  |
| <b>Author notification:</b>        | <b>July 23, 2027</b> |

We also seek proposals for panels and special sessions; please reach out to the Program Chair for more information. Test Week tutorial and workshop proposals are also welcomed. Deadlines and other information about proposals can be obtained from TTTC at: <http://tab.computer.org/tttc>

For further information, please consult the ITC website at <http://www.itctestweek.org> or contact the chairs below.

**Sandeep Kumar Goel**  
**General Chair**  
TSMC  
skgoel (AT) tsmc.com

**Hung-Pin (Charles) Wen**  
**Program Chair**  
NYCU  
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*ITC invites submissions on the latest advances in test, validation, diagnosis, implementation, and scalability for ICs, boards, and systems, covering cross-domain, test economics, and product lifecycle challenges.*

**Topics of interest include, but not limited to**

### Test Methodologies & Technologies

- Adaptive Test in Practice
- ATE & Probe Card Design
- Built-In Self-Test (BIST)
- Boundary Scan & JTAG
- Design for Test (DFT) & DFM
- Mixed-Signal & Analog Test
- Memory Test & Repair
- MEMS Testing
- Power Issues in Test
- High-Speed I/O, RF & Jitter Test
- Test Compression & Optimization
- Test Generation & Validation

### Industrial Case Study & Application Test

- 3D/2.5D & Advanced Packaging
- SoC/NoC Test
- Hardware Security & Trust
- Automotive and IoT Test
- System Test
- Silicon case studies

### Verification, Debug & Analysis

- Pre-Silicon/Post-Silicon Verification
- Silicon Debug & Field Monitoring
- Diagnosis & Defect Analysis
- Data-Driven Test & End-to-End Analytics
- Yield Analysis & Optimization
- Test-to-Design Feedback & Escape Analysis

### Emerging Topics

- Reliability & Resilience
- Emerging Defect Mechanisms
- Protocol-Aware Test
- Quantum Device Testing
- KGD/KGS/KGP Economics
- New Technologies & Standards

### Large AI Systems & Shared Silicon Challenges

- AI Accelerator, HBM & Chiplet Test
- Wafer-Scale & System-Level Test

### AI for Test Efficiency & Innovation

- LLM- & Agent-Assisted Test
- AI-Driven Diagnosis & Test Flows

