2026 INTERNATIONAL TEST CONFERENCE

OCTOBER 11 - 16, 2026

Grand Hyatt San Antonio Riverwalk, TX, USA

Call for Papers

The International Test Conference (ITC) is the world's premier forum for the electronic test of devices, boards, and systems, covering the entire product lifecycle from design verification to process improvement. The test landscape is rapidly evolving. Emerging manufacturing technologies, the pervasive influence of AI, and the critical need for trustworthy devices present both challenges and opportunities for off-chip and on-chip test. This includes the demand for cost-effective testing of large AI systems and robust solutions for stringent quality requirements in applications like automotive. Test inherently sits at the crossroads of multiple disciplines, influencing and being influenced by design, manufacturing, and PPA. We are also at an industrial inflection point, with AI disrupting our traditional approaches to test.

We invite authors to submit original, unpublished papers describing recent work in testing and testable design. Of particular interest are contributions addressing the topics listed in this call for papers and/or those focused on our specialized tracks. **This year, we are particularly excited to introduce two new tracks:**

Track A: Large AI Systems & Shared Silicon Challenges: This track focuses on the unique test and implementation challenges of large-scale AI chips, covering architecture, advanced packaging, PPA optimization, and test cost effectiveness.

Track B: AI for Test Efficiency & Innovation: This track explores innovative applications of AI and Machine Learning (including LLMs) to enhance test efficiency, automate design verification, improve diagnostics, and optimize the overall test flow.

These contributions should enable the wider community to learn from and adopt best industrial practices, sharing real-world insights and solutions.

Submissions must include:

- Title of paper.
- Name, affiliation, e-mail address of each author.
- The corresponding author(s). ITC will communicate with the corresponding author(s).
- One or two topic(s) from the topic list, or a description of your topic.
- An electronic copy of a complete paper of up to 10 pages and an abstract of 100 words or less to be entered online.

Important Note: ITC maintains a competitive selection process. Submissions must clearly describe the work's status, contribution, novelty, and significance. Papers under simultaneous review or already accepted by another conference will be summarily rejected. Submissions shorter than 4 pages are rarely accepted. For AI-focused papers, an appendix of up to 6 pages may be submitted in addition to the main paper.

Paper title/abstract due:	**March 20, 2026**
Paper final PDF due:	**April 24, 2026**
Author notification:	**June 19, 2026**

We also welcome single-page poster proposals for late-breaking results, innovative methods seeking feedback, or participation without a full paper. Poster acceptance does not prevent future submission as an ITC paper in 2027. More information on posters will be provided on the ITC webpage.

Poster submission deadline:	**July 10, 2026**
Author notification:	**July 24, 2026**

Test Week tutorial and workshop proposals are also welcomed. Deadlines and other information about proposals can be obtained from TTTC at: http://tab.computer.org/tttc

For detailed information about the submission process, requirements and deadlines, the selection process and any other questions regarding the program itself or contact information, please consult the ITC web site at http://www.itctestweek.org.

ITC invites submissions on the latest advances in test, validation, diagnosis, implementation, and scalability for ICs, boards, and systems, covering cross-domain, test economics, and product lifecycle challenges.

Topics of interest include, but not limited to

Test Methodologies & Technologies

- Adaptive Test in Practice
- ATE & Probe Card Design
- Built-In Self-Test (BIST)
- Boundary Scan & JTAG
- Design for Test (DFT) & DFM
- Mixed-Signal & Analog Test
- Memory Test & Repair
- MEMS Testing
- Power Issues in Test
- High-Speed I/O, RF & Jitter Test
- Test Compression & Optimization
- Test Generation & Validation

Industrial Case Study, System, & Application Specific Test

- 3D/2.5D & Advanced Packaging
- SoC/NoC Test
- 5G/6G Test
- Hardware Security & Trust
- Automotive Test
- IoT Test
- System Test
- Silicon case studies

Verification, Debug & Analysis

- Pre-Silicon/Post-Silicon Verification
- Silicon Debug & Field Monitoring
- Diagnosis & Defect Analysis
- Data-Driven Test & End-to-End Analytics
- Yield Analysis & Optimization
- Test-to-Design Feedback & Escape Analysis

Emerging Topics

- Reliability & Resilience
- Emerging Defect Mechanisms
- Protocol-Aware Test
- Optics & Photonics Test
- AI/Machine Learning in Test
- Quantum Device Testing
- KGD/KGS/KGP Economics
- New Technologies & Standards

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