ITC 2016 P X #: Testing Yield Improvement by Optimizing the Impedance of Power Delivery Network on DIB

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Scan Test Challenges Caused by IR Drop

1. Transition delay at-speed tests are sensitive to IR drops on the power supplies
2. Impedances of Power Delivery Network (PDN) on Device Interface Board (DIB) have big impact on the IR drop
3. In multi-site testing, different sites may have different PDN impedances vs. frequencies due to variations of layout traces or capacitance values
4. Multi-site testing may introduce even larger yield loss due to variations of IR drops on PDNs

Shmoo of the Same Device on 8 Different Sites

Proposed Flow

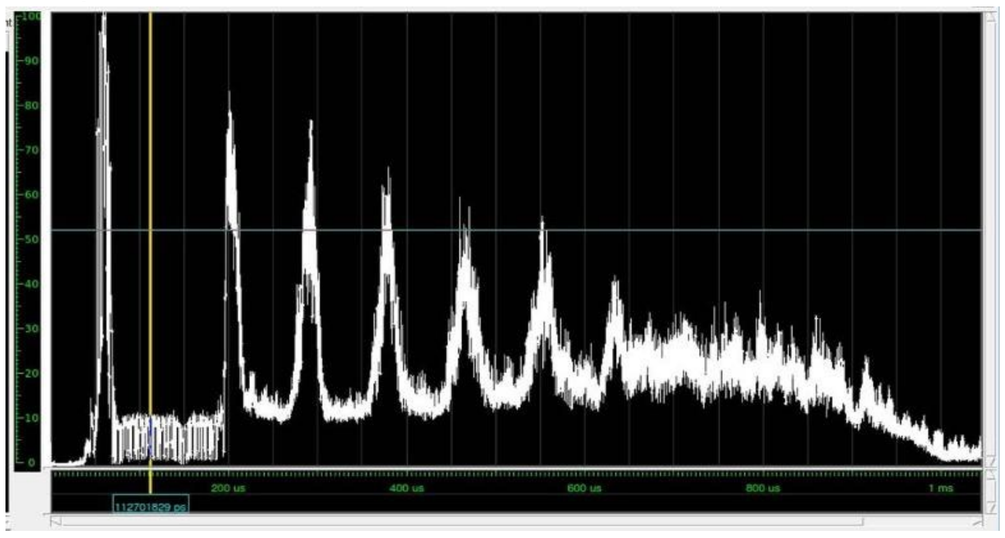
Step 1. Analyze test power to identify sensitive frequencies and calculate the impedance thresholds at these points

Step 2. Measure how PDN impedances vary with frequencies at different test sites

Step 3. Optimize the PDN impedance if it is over the threshold

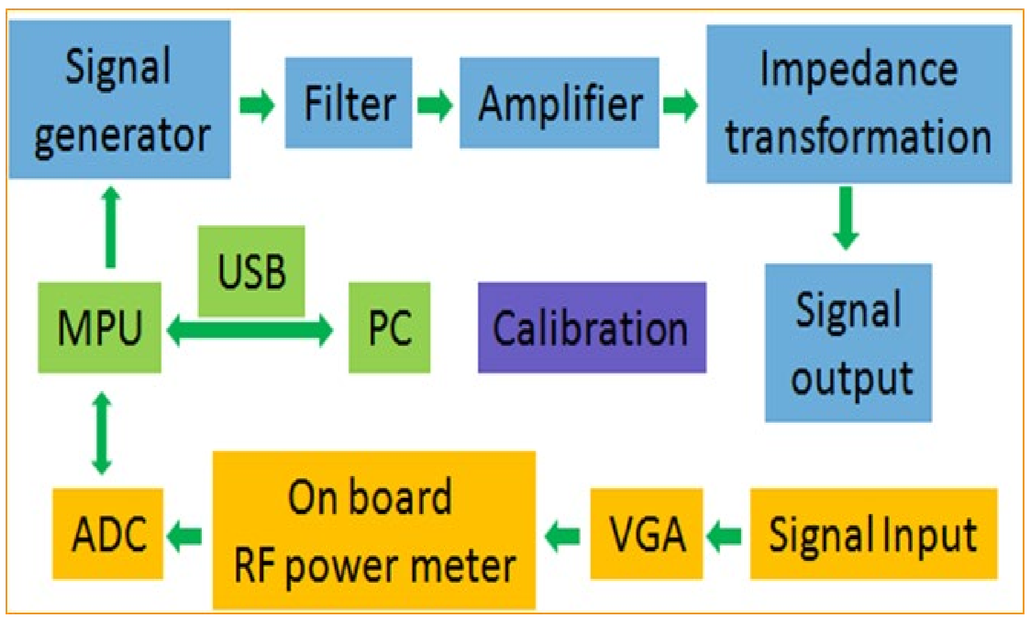
Step 1: Analyze

Identify the sensitive frequency points, at which the worst IR drops may happen. The following is an example of peak power analysis results based on simulation.

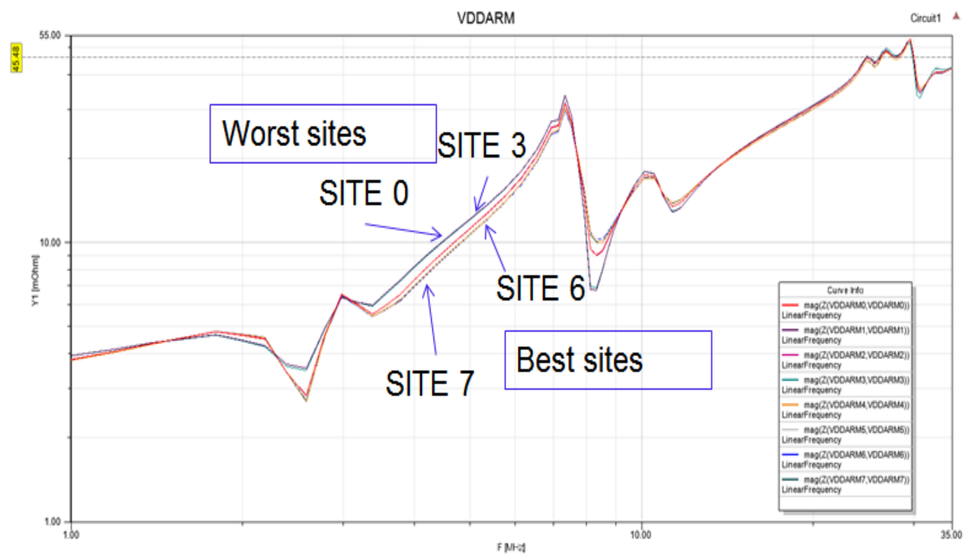


Step 2: Measure

A circuit is developed to scan the PDN impedance on each site. Its block diagram is illustrated as follows



With the designed circuitry, we measure the impedance vs. the frequency. In this example, the best sites are Sites 6 and 7 and the worst sites are Sites 0 and 3, which matched the shmoo results



Step 3: Optimize

If at some sensitive frequencies, the measured impedance is larger than the calculated threshold, we will tune the capacitances on the PDN such that its impedance will drop to a safe level and IR drop will not likely occur. This can minimize yield loss due to IR drops.