General Instructions for ITC 2025 Posters

This file contains instructions to prepare and upload your poster-related files. Please read all instructions carefully.

1. **Poster exposition:** All posters will be exposed along the entire ITC25 conference; **posters' authors have to tag their printed posters during the first conference day**. The poster stand number # can be found in the smart easychair program at https://easychair.org/smart-program/ITC2025/ in the poster session description. Also, posters' session and # can be found in the table at the end of this file.
2. **Poster presentation:** there will be two sessions held from **12:00 p.m.– 01:30 p.m.**, on **Wednesday, September 24th** and **Thursday, September 25th** (kindly check the official ITC website for detailed information and the table below), on the exhibition floor of ITC 2025. Note that the posters should be hung anytime Wednesday.
3. **MANDATORY Poster format:** please prepare a **A1-sized poster**, **59.4 cm x 84.1 cm,** or approximately **24 inches x 36 inches, portrait orientation** (84.1 cm / 36 inches in height). Samples or guidelines for posters can be found at http://www.itctestweek.org/itc-authors-page/.
4. **Printing poster:**
   - (Default) **Print it by yourself** and bring it to the conference site,
   - (Option) ITC uses **Pinnacle Exposition Services LLC** (web: **https://pinnacle-expo.com** / email: **jpelton@pinnacle-expo.com** / phone: **1-919-756-9924**) to print banners. If you want to use them to print poster, please contact Pinnacle Exposition Services LLC directly. ITC does **NOT** provide the printing service. If you use their service, your poster will be shipped with other ITC banners to the conference site.
   - (Option) You can also find a local print service (e.g. Fedex office at San Diego downtown – please google) and use them. If you use a local service like this, you can pick it up yourself and bring it to the exhibit floor to set up the poster. ITC does **NOT** provide any pick-up service.
5. **File name:** We also ask you to upload your poster file for it to be included in the ITC website. Please start the file name as "**Poster_X_#.pdf**". Replace X with the poster session (1 or 2), # with your poster stand number #. Your poster ID can be found in the table at the end of this file.
6. **Submission link:** The link to upload your poster is given below, where you will also be requested to fill in your information and a release consent form.

   https://forms.gle/H5HG81K4FtTMnVvA6

   The deadline (firm) for filling out the form and uploading your poster file is **September 15th, 2025.** Because we will have a physical poster session, each poster presenter needs to present in person during the session.
7. **Registration**:

- All poster presenters must register ITC under the "**ITC Technical Conference Program Participant**" category. All presenters are expected to be physically present during the poster session on the exhibit floor.
- The advance registration deadline is **July 31st, 2025**.
- A limited number of rooms in the hotel are available exclusively for ITC 2025 participants. The hotel booking deadline is also **July 31st, 2025**. After the deadline, the hotel will NOT honor the ITC hotel rate any more.

List of Posters in ITC 2025

POSTER SESSION 1: 12:00 p.m.– 01:30 p.m., Wednesday, September 24th

Poster stand #	Title	Authors
1	5G RF Test Interface Diagnosis in Automatic Test Equipment (ATE)	Hsuan-Yin Huang, Ching-Nen Peng and Kuo-An Wang
4	Device-Aware Test for Threshold Voltage Shifting in FeFET	Changhao Wang, Sicong Yuan, Hanzhi Xun, Nicolo Bellarmino, Danyang Chen, Chujun Yin, Mottaqiallah Taouil, Moritz Fieback, Xiuyan Li, Lin Wang, Chaobo Li, Riccardo Cantoro, Said Hamdioui and Nima Kolahimahmoudi
5	Early Testing of Memory Redundant Row Elements	Luc Romain, Albert Au, Roger Mah, Katarzyna Wojnowska and Lori Schramm
8	Eclipse Dynamic Probe Card: A Novel Approach for Wafer-Level Photonic Testing with Automated Fiber Array Unit Alignment	Alessia Galli and Riccardo Vettori
9	Exploiting the correlation with traditional fault models to speed-up cell-aware ATPG	Reza Khoshzaban, Riccardo Cantoro, Matteo Sonza Reorda, Michelangelo Grosso and Iacopo Guglielminetti
12	Influence of Automated Test Equipment Drift on Process Capability Studies	Anand Venkatachalam, Ernst Aderholz, Matthias Sauer, Simon Schweizer, Matthias Werner and Ilia Polian
13	An On-Chip Sensor For Online Monitoring of HCI-Induced Aging In Integrated Circuits	Saeid Karimpour, Emmanuel Nti Darko and Degang Chen
16	Accelerate Verification, Streamline Challenges: A Comprehensive High Bandwidth Memory (HBM) Solution	Vatsal Patel, Ritesh Desai, Ujash Poshiya and Dharini Subashchandran
17	Advancing ATE for EV Battery Management: Overcoming Test Challenges with Smart Solutions	Sandeep D'Souza, Matthew Getz and Tim Bakken
20	Early Reliability Estimation in Hardware Accelerators through an Improved Colored Petri Net Approach	Ernesto Cristopher Villegas Castillo, Josie Esteban Rodriguez Condia, Juan-David Guerrero-Balaguera, Felipe Augusto da Silva and Michael Glass
21	Consistency verification between the iJTAG network and its ICL description with optimized simulation time, ease of debuggability and test completeness	Divyank Mittal, Sagar Kumar, Sameer Chillarige and Jyotirmoy Saikia
24	FAMOUS: Fault Attack Mitigation via Exploiting Invariances in Deep Neural Networks	Javad Bahrami, Parsa Nooralinejad, Hamed Pirsiavash and Naghmeh Karimi

25	Dynamic SCAN Shift in High Volume Manufacturing Testing for Test Time Optimization	Lim Mao Ding, Yu Tin Cheong, Khai Wern Heng and Li Sok Khor
28	FPGA Synthesis of Arbitrary Jitter Injection for Multi-GHz Test Signals	Shengbo Liu, Xiao Yindong, Cao Wang, Xiaochun Li and David Keezer
29	Hierarchical Test Using Running MISR Signatures	Brion Keller, Dale Meehl, Krishna Chakravadhanula and Pradeep Nagaraj
32	High Reliability Delay-Based Weak FPGA PUF Using High-Resolution Stochastic Delay Measurement With Phase Locked Loops	Kentaroh Katoh, Toru Nakura and Haruo Kobayashi
33	Low Noise 20-bit DAC for ATE	Brian Friend, Neha Udaiwal and Marzio Pedrali-Noy
36	Method for Diagnosing Clock Jitter Using FPGA	Seongkwan Lee, Hyuntae Jeong, Cheolmin Park, Jun Yeon Won, Minho Kang and Jaemoo Choi
37	Minimal Supervision, Maximum Accuracy: TabPFN for Microcontroller Performance Prediction	NicolÃ² Bellarmino, Riccardo Cantoro, Martin Huch and Tobias Kilian
40	MUX-based Polymorphic Registers and FSMs to Protect Against Non-invasive Voltage Fault Injection Attacks	Sourav Roy and Domenic Forte
41	Improving Deterministic Test Pattern Generation through Massive Static Learning	Peter Wohl, Jonathon Colburn, John Waicukauski and Yasunari Kanzawa
44	Experimental Comparison of Multiplexing Methods for 28 to 64 Gbps NRZ Test Signals	Cao Wang, Shengbo Liu, Ming Cheng, Yindong Xiao, Xiaochun Li and David Keezer
45	DMA Burst Mode Fault Detection: Custom MBIST Strategies for Comprehensive Testing	Prakash Kumar, Ratheesh Thekke Veetil and Ajay Purushotham
48	FeTest: Testing of FeFET-Based Memory Arrays	Dhruv Thapar, Arjun Chaudhuri, Kai Ni and Krishnendu Chakrabarty
49	Enhancing scan coverage in mixed signal designs by clock and reset manipulation during testing	Khushboo Agarwal, Ari Shtulman, Ahmet Tokuz, Hoang Nguyen and Manjushree Shivarudraiah
52	Graph Attention Network Based Fault Prediction Framework for Functional Safety Verification	Yutao Sun, Jiehua Huang, Xiangping Liao, Zhijun Wang and Liping Liang
53	High performance advanced fault model diagnosis	Bharath Nandakumar, Sameer Chillarige and Vaibhav Mishra
56	Combined Array and ADC Structural Test for RRAM-based Multiply-and-accumulate Circuits	Emmanouil Anastasios Serlis, Hanzhi Xun, Emmanouil Arapidis, Anteneh Gebregiorgis, Mottaqiallah Taouil, Said Hamdioui and Moritz Fieback
57	AMBA Qchannel based power management VIP for Efficient low power validation	Gokul T and Raveendranath Reddy P
60	Deep Learning-based IC Monitoring	Iresh Jayawardana Manannaidelage, Krishna Dahal, Spyros Tragoudas, Khader Abdel Hafez and Danushka Senarathna
61	Autonomously access 1687 instruments with Controllable ScanRegisters and ScanMuxes at top level with AccessLink	Kshitij Kulshreshtha, Vistrita Tyagi, Shrutika Patil, Manish Arora, Deepika Reddy Yenna and Shamitha Rao
64	Assessment of System-Level Test programs in Automotive SoCs	Giusy Iaria, Claudia Bertani and Vincenzo Tancorre

POSTER SESSION 2: 12:00 p.m.– 01:30 p.m., Thursday, September 25th

Poster stand #	Title	Authors
2	An SMT-Based Method for Identifying State-Holding Elements in Extracted Netlists	Aric Fowler, Carl Sechen and Yiorgos Makris
3	CP-Bench: A PyTorch Test Suite to Detect AI Hardware Failure, Performance Degradation, and Silent Data Corruption	Xun Jiao, Fred Lin, Sunny Yang, Suman Gumudavelli, Shreya Varshini, Harish Dixit, Abhinav Pandey, Ahbinav Jauhri, Tyler Graf, Francesco Caggioni, Venkat Ramesh, Philip Henzler, Sameeksha Gupta, Jason Liang and Gautham Vunnam
6	Embedded Trace: A Key Enabler for Silicon Lifecycle Management	Vivek Chickermane, Marcel Zak and Mat O'Donnell
7	Functional Logic Diagnosis with Observation Points on Next-State Variables	Irith Pomeranz
10	Glitter PUF: A Passive Anti-Tamper PUF Based On Images Of Glitter Reflection	NoeÃ«l Moeskops, Abdullah Aljuffri, Said Hamdioui and Mottaqiallah Taouil
11	Scan Strategies for High Quality Latch Array Testing	Bin Du, Nehal Patel, Yerong Chen, Jeremy Chin and Kethreine Tian
14	Improving Error Tolerance and Scalability in Pseudo-Boolean SAT-based Generic Side-Channel Analysis	Shakil Ahmed, Dipali Jain and Kaveh Shamsi
15	In-Field Testing using In-System Embedded Deterministic Test as a solution to alleviate Silent Data Corruption in AI designs	Ashrith S Harith, Subramanian Mahadevan, Nilanjan Mukherjee, Varun Sehgal, Saket Goyal and Mohit Sharma
18	Wafer Map Pattern Recognition using Ternary Spiking Neural Network	Abhishek Kumar Mishra, Anup Das and Nagarajan Kandasamy
19	Test Pattern Aware Streaming Fabric-based Scan Test Methodology	Krishna Gnawali, Andrea Costa, Nathalie Etono, Denis Martin, Bala Tarun Nelapatla and Amit Purohit
22	Optimizing Sensing Point Placement for High-Multi-Site Testing on Device Interface Boards	Ashley Chien-Hui Huang, Derek Hong-Yi Yang and Siya Ssu-Ya Liao
23	Wafer Map Pattern Recognition for Multisite Probe with Synthetic Data Augmented Training	Chen He, Rebecca Chen and Patrick Goertz
26	Teaching Llamas to Test: A Large Language Model-Based Approach	Christos Vasileiou and Yiorgos Makris
27	Resurgence in Advanced ATPG Techniques for High-Performance Designs	Dale Meehl, Krishna Chakravadhanula, Brion Keller and Pradeep Nagaraj
30	TIDE: Telemetry-Informed Delay Testing for Silent Data Corruption	Deepesh Sahoo, Eduardo Ortega, Peter Domanski, Farshad Firouzi and Krishnendu Chakrabarty
31	Statistical Analysis of the Nonlinearity Errors of Unary and Binary-Weighted DACs	Godfred Bonsu, Isaac Bruce, Emmanuel Darko, Kelvin Tamakloe and Degang Chen
34	Machine Learning Assisted Vmin Prediction	Huitong Chen, Xinyu Sun, Rongrong Liu, Robert Wu and Kashish Shah
35	Secure and Efficient Sharing of On-Chip Resources	Joel Ã…hlund, Markus TÃ¶rmÃ¤nen and Erik Larsson
38	Structural Testing on SLT Platform with HSAT IP & High-Speed I/O Access	Jyotika Suri, Rakesh Kinger, Sridhar Nimmagadda and Henry Fei

39	Precise Approach to ATPG: Handling Timing Exceptions for Better Small Delay Defect Coverage	Lana Pantskalashvili, Ron Press and Hans Tsai
42	STARTS: Simulation Traits Assisted Random Test Selection for Multiprocessor Verification	Li Zhou, Menglong Lu, Li Luo, Jianfeng Zhang and Junbo Tie
43	Sharing Scan Bandwidth Across Die to Die in MCM Package	Manish Bhattarai, Ramu Setty and Manish Bhattarai
46	Origen Based Test and Validation	Paul DeRouen and Joe Chayachinda
47	Test and Calibration Methods for Process Variation of ReRAM-based Spiking Neural Networks	Po-Sheng Chiu, Chih-Yu Hsu, Chih-Tsun Huang and Jing-Jia Liou
50	Test Bin Entitlement: Yield Outlier Detection using Die Area and LLM based Bin-Grouping	Ragad Al-Huq and Yuegui Zheng
51	Why is Rigorous PCIe Interoperability Testing is Key to Robust and Reliable Systems?	Sean Chen, Frank Chang, Victor Castillo, Amarildo Garcia and Joe Obedowski
54	Testing of Passive Memristor Crossbars in AI Hardware Accelerators	Shanmukha Mangadahalli Siddaramu, Mahta Mayahinia, Surendra Hemaram and Mehdi Tahoori
55	Platform Thermal Management in System Level Test: Analysis of existing solutions and introduction to advanced liquid cooled memory solutions	Sridutt Tummalapalli and Srinath Reddy Yerakondappagari
58	Most Effective At-Speed Test: Hybrid Launch-Off-Shift and Capture Technique	Takeo Kobayashi, Ron Press and Lana Pantskalashvili
59	Methodology for Accurate and Automated IDD Characterization on ATE	Todd Jacobs and Peter Smykla
62	The Role SLT Plays at Intel	Vishwanath Natarajan, Carlos O Bernabe and Ethan Hansen
63	IEEE P1450.6.2: Core Test Language (CTL) for Memories An update to the existing standard	Saman Adham, Puneet Arora, Albert Au and Artur Pogiel