



# 2025 INTERNATIONAL TEST CONFERENCE

September 21 - 26, 2025

SAN DIEGO, CA, USA

## Call for Informal Posters

The International Test Conference (ITC) is the world's premier venue dedicated to the electronic test of devices, boards and systems—covering the complete cycle from design verification, design- for-test, design-for-manufacturing, silicon debug, manufacturing test, system test, diagnosis, reliability and failure analysis, and back to process and design improvement.

Authors are invited to submit original, unpublished papers describing recent work in the field of testing and testable design. Of particular interest are works dedicated to the topics listed on the right and/or works focused on special tracks such as **Automotive Reliability, Reliability of AI HW and usage of AI for Testing, 3D/2.5D and Chiplet Testing, or HW Security**. Authors are also invited to submit practical, industry-oriented papers.

### Submissions must include:

- Title of paper.
- Name, affiliation, e-mail address of each author. (Double blind review is not required).
- The corresponding author(s). ITC will communicate with the corresponding author(s).
- An electronic copy of a complete paper of **1 page**.
- An abstract of 110 words or less to be entered online.

Posters are a useful way of presenting late-breaking results, getting feedback on an innovative method, or participating without having to write a full paper. Acceptance as a poster does not preclude submission of a more complete work as an ITC paper in 2026. Additional information on poster submissions will be provided on the ITC web page.

**Poster submission deadline:**

**May 20, 2025**

**Author notification:**

**June 15, 2025**

Presenters of accepted informal posters are invited to prepare a poster to present during poster sessions at ITC25. Optionally, the 1-page paper could be linked to the ITC website, upon authorization from the authors.

Test Week tutorial and workshop proposals are also welcomed. Deadlines and other information about proposals can be obtained from TTTC at: <http://tab.computer.org/tttc>

**For detailed information** about the submission process, requirements and deadlines, the selection process, and any other questions regarding the program itself or contact information, please consult the ITC web site at <http://www.itctestweek.org>.

For further information:

### General Chair

**Jennifer Dworak**

Southern Methodist University, US

[jdworak@smu.edu](mailto:jdworak@smu.edu)

### Program Chair

**Paolo Bernardi**

Politecnico di Torino, IT

[paolo.bernardi@polito.it](mailto:paolo.bernardi@polito.it)

*ITC invites submissions on the latest advances in test, validation, diagnosis and security of IPs, ICs, boards and systems.*

### Topics of interest include, but not limited to:

3D/2.5D Test  
5G/6G Test  
Adaptive Test in Practice  
AI/Machine Learning in Test  
ATE/Probe Card Design  
Automotive Reliability  
Advances in Boundary Scan  
Built-In Self-Test  
Data Driven Test Methods  
Defect-oriented Testing  
Design for Test (DFT)  
DFM and Test  
Diagnosis  
Economics of Test  
End-to-End Data Analysis  
End-to-End System Security  
Emerging Defect Mechanisms  
Field Monitoring, Test, & Debug  
Hardware Security and Trust  
IoT Testing  
Jitter, High-Speed I/O and RF Test  
Known-Good-Die Test  
Memory Test and Repair  
MEMS Testing  
Mixed-Signal and Analog Test  
New Technologies and Test  
Online Test  
Pre-Silicon/Post-Silicon Verification  
Power Issues in Test  
Protocol-aware Test  
Quantum Device Testing  
Reliability and Resilience  
SoC/SiP/NoC Test  
Silent Data Corruption  
Silicon Debug  
Simulation and Emulation  
System Test (Applications)  
System Test (Hardware/Software)  
Test Compression  
Test-to-Design Feedback  
Test Escape Analysis  
Test Flow Optimizations  
Test Generation and Validation  
Test Resource Partitioning  
Test Standards  
Testing High Speed Optics/Photonics  
Timing Test  
Yield Analysis and Optimization

