



2025 INTERNATIONAL TEST CONFERENCE

September 21 - 26, 2025
SAN DIEGO, CA, USA

Call for Papers

The International Test Conference (ITC) is the world's premier venue dedicated to the electronic test of devices, boards and systems—covering the complete cycle from design verification, design- for-test, design-for-manufacturing, silicon debug, manufacturing test, system test, diagnosis, reliability and failure analysis, and back to process and design improvement.

Authors are invited to submit original, unpublished papers describing recent work in the field of testing and testable design. Of particular interest are works dedicated to the topics listed on the right and/or works focused on special tracks such as **Automotive Reliability, Reliability of AI HW and usage of AI for Testing, 3D/2.5D and Chiplet Testing, or HW Security**. Authors are also invited to submit practical, industry-oriented papers.

A **special industrial case-study track** is dedicated to papers that enable others to learn best industrial practices.

Submissions must include:

- Title of paper.
- Name, affiliation, e-mail address of each author. (Double blind review is not required).
- The corresponding author(s). ITC will communicate with the corresponding author(s).
- One or two topic(s) from the topic list, or a description of your topic.
- An electronic copy of a complete paper of 6~10 pages for regular papers (including regular Industrial case-study papers) or 3~5 pages for short Industrial Practices papers.
- An abstract of maximum 100 words to be entered online.

ITC maintains a competitive selection process for technical papers. Submissions must clearly describe the status of the reported work, its contribution, novelty and/or significance. Supporting data, results (priority is often given to papers with results from real designs) and conclusions, and references to prior work must also be included.

Paper title/abstract due: **March 7, 2025**
Paper PDF due: **April 5, 2025, 11:59 PM PDT (Extended)**
Author notification: **May 13, 2025**
Final manuscript due: **June 15, 2025**

Test Week tutorial and workshop proposals are also welcomed. Deadlines and other information about proposals can be obtained from TTTC at: <http://tab.computer.org/tttc>

For detailed information about the submission process, requirements and deadlines, the selection process, and any other questions regarding the program itself or contact information, please consult the ITC web site at <http://www.itctestweek.org>.

For further information:

General Chair

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Program Chair

Paolo Bernardi

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Topics of interest include, but not limited to:

3D/2.5D Test	Mixed-Signal and Analog Test
5G/6G Test	New Technologies and Test
Adaptive Test in Practice	Online Test
AI/Machine Learning in Test	Pre-Silicon/Post-Silicon
ATE/Probe Card Design	Verification Power Issues in Test
Automotive Reliability	Protocol-aware Test
Advances in Boundary Scan	Quantum Device Testing
Built-In Self-Test	Reliability and Resilience
Data Driven Test Methods	SoC/SiP/NoC Test
Defect-oriented Testing	Silent Data Corruption
Design for Test (DFT)	Silicon Debug
DFM and Test Diagnosis	Simulation and Emulation
Diagnosis	System Test (Applications)
Economics of Test	System Test (Hardware/Software)
End-to-End Data Analysis	Test Compression
End-to-End System Security	Test-to-Design Feedback
Emerging Defect Mechanisms	Test Escape Analysis
Field Monitoring, Test, & Debug	Test Flow Optimizations
Hardware Security and Trust	Test Generation and Validation
IoT Testing	Test Resource Partitioning
Jitter, High-Speed I/O and RF	Test Standards
Test Known-Good-Die Test	Testing High Speed Optics/Photonics
Memory Test and Repair	Timing Test
MEMS Testing	Yield Analysis and Optimization

Program committee members:

P. Bernardi, PoliTO (Program Chair)	S. Banerjee, Meta (Past Program Chair)
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A. Ruospo, PoliTO	A. Sinha, Intel
M. Sonza Reorda, PoliTO	P. Song, IBM
F. Su, Intel	H.-G. Stratigopoulos, CNRS
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