2024 INTERNATIONAL TEST CONFERENCE

NOVEMBER 3 - 8, 2024
SAN DIEGO, CA, USA

Call for Papers

The International Test Conference (ITC) is the world's premier venue dedicated to the electronic test of devices, boards and systems—covering the complete cycle from design verification, design-for-test, design-for-manufacturing, silicon debug, manufacturing test, system test, diagnosis, reliability and failure analysis, and back to process and design improvement.

Emerging technologies in design and manufacturing will require new test solutions. Artificial Intelligence (AI) and the need for trustworthy devices are providing both new challenges and new opportunities for off-chip and on-chip test. At the same time, more stringent quality requirements, especially in automotive applications, are requiring more efficient test, debug, monitoring, and repair techniques that can transfer to the field.

Authors are invited to submit original, unpublished papers describing recent work in the field of testing and testable design. Of particular interest are works dedicated to the topics listed on the right and/or works focused on special tracks such as Automotive, 5G/6G, AI, or Security. Authors are also invited to submit practical, industry-oriented papers. A special **industrial case-study track** is dedicated to papers that enable others to learn best industrial practices. Submissions simultaneously under review or accepted by another conference, symposium or journal, will be summarily rejected. The submission is through the Easychair paper submission system - https://easychair.org/conferences/?conf=ieeeitc2024.

Submissions must include:

- Title of paper.
- Name, affiliation, e-mail address of each author.
- The corresponding author(s). ITC will communicate with the corresponding author(s).
- One or two topic(s) from the topic list, or a description of your topic.
- An electronic copy of a complete paper of 6~10 pages for regular papers (including Industrial case-study papers) or 3~5 pages for short Industrial Practices papers.
- An abstract of 35 words or less to be entered online.

ITC maintains a competitive selection process for technical papers. Submissions must clearly describe the status of the reported work, its contribution, novelty and/or significance. Supporting data, results (priority is often given to papers with results from real designs) and conclusions, and references to prior work must also be included. ITC does not accept submissions that do not meet the specified criteria.

Paper title/abstract due:	**April 19, 2024**
Paper PDF due:	**April 26, 2024**
Author notification:	**June 14, 2024**
Final manuscript due:	**August 30, 2024**

Authors are also invited to submit a **single-page** poster proposal. Posters are a useful way of presenting late-breaking results, getting feedback on an innovative method, or participating without having to write a full paper. Acceptance as a poster does not preclude submission of a more complete work as an ITC paper in 2025. Additional information on poster submissions will be provided on the ITC web page.

Poster submission deadline:	**June 28, 2024**
Author notification:	**July 9, 2024**

Test Week tutorial and workshop proposals are also welcomed. Deadlines and other information about proposals can be obtained from TTTC at: http://tab.computer.org/tttc

For detailed information about the submission process, requirements and deadlines, the selection process and any other questions regarding the program itself or contact information, please consult the ITC web site at http://www.itctestweek.org.

ITC invites submissions on the latest advances in test, validation, diagnosis and security of IPs, ICs, boards and systems.

Topics of interest include, but not limited to:

3D/2.5D Test
5G/6G Test
Adaptive Test in Practice
AI/Machine Learning in Test
ATE/Probe Card Design
Automotive Test
Advances in Boundary Scan
Built-In Self-Test
Data Driven Test Methods
Defect-oriented Testing
Design for Test
DFM and Test
Diagnosis
Economics of Test
End-to-End Data Analysis
End-to-End System Security
Emerging Defect Mechanisms
Field Monitoring, Test, & Debug
Hardware Security and Trust
IoT Testing
Jitter, High-Speed I/O and RF Test
Known-Good-Die Test
Memory Test and Repair
MEMS Testing
Mixed-Signal and Analog Test
New Technologies and Test
Online Test
Pre-Silicon/Post-Silicon Verification
Power Issues in Test
Protocol-aware Test
Quantum Device Testing
Reliability and Resilience
SoC/SiP/NoC Test
Silicon Debug
Simulation and Emulation
System Test (Applications)
System Test (Hardware/Software)
Test Compression
Test-to-Design Feedback
Test Escape Analysis
Test Flow Optimizations
Test Generation and Validation
Test Resource Partitioning
Test Standards
Testing High Speed Optics/Photonics
Timing Test
Yield Analysis and Optimization

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