General Author Instructions for ITC 2023 Posters

This file contains instructions to prepare and upload your poster-related files. Please read all instructions carefully.

1. **Poster session time and place:** The poster session will be held from **12:00 p.m.–02:00 p.m.**, **October 11 (Wednesday) 2023**, on the exhibition floor of ITC 2023.
2. **Poster size:** About **3' x 4'** (90.7 cm by 121 cm) in **portrait** orientation.
3. **Items to be uploaded:** Below is the list of required and optional items for posters. Because we will have a physical poster session, each poster presenter needs to present in person during the session.
   - (**Required**) A 1-page **3'x4' portrait poster (4' in height)** (PDF).
   - (Encouraged) A **1-to-2-page paper document** (PDF). It should follow IEEE 2-column conference format (https://www.ieee.org/conferences/publishing/templates.html). Note that this paper will be hosted by ITC virtual site hosted by Underline.
   - (Encouraged) A **2-to-5-minute preview video** (MP4) to be put on the virtual site of ITC and can be seen online before/during/after the conference.

   Samples or guidelines for posters and poster papers are can be found at http://www.itctestweek.org/itc-authors-page/. There is ***no set format*** for the **preview video**. Use your creativity to prepare the video that can attract people to your poster.
4. **File names:** In each uploaded file, please start the file name with your poster ID, such as "PO.3 poster", "PO.3 paper," and "PO.3 video" where your poster ID can be found in the table attached at the end of this file. If you want to upload the optional 1-or-2-page paper-format document, please use the provided template file "ITC-poster-paper-template." On the bottom line of the template, you can see "Poster X." Please replace X with your poster ID.
5. **Submission link:** The link to upload your files is given below, where you will also be requested to fill in your information and a release consent form.

   https://itc2023presenterform.paperform.co/

   Even though the link is accessible now, please do **NOT** submit your files yet. Please **wait for a go-ahead** message from the ITC Program Office before submitting them.

   The deadline for filling out the form and uploading all files is **September 15, 2023.** This deadline is firm.

6. **Printing posters:**
   - (Default) Print it by yourself and bring it to the conference site,
   - (Option) ITC uses **Pinnacle Exposition Services LLC** (web: https://pinnacle-expo.com / email: posters@pinnacle-expo.com / phone: **1-855-451-6893**) to print banners. If you want to use them to print poster, please contact Pinnacle Exposition Services LLC directly. ITC does **NOT** provide the printing service. If you use their service, your poster will be shipped with other ITC banners to the conference site.

- (Option) You can also find a local print service (e.g. Fedex office at Anaheim downtown – please google) and use them. Note: If you use Fedex service, you would select “mounted poster” with the size 36”X48’’ “extra large portrait”. If you use a local service like this, you can pick it up yourself and bring it to the exhibit floor to set up the poster. ITC does **NOT** provide any pick-up service.

7. **Registration:**
   - All poster presenters must register ITC under the “**Program Participant**” category. All presenters are expected to be physically present during the poster session on the exhibit floor.
   - The advance registration deadline is September 1st, 2023.
   - The hotel booking deadline is also September 1st, 2023. After the deadline, the hotel will **NOT** honor the ITC hotel rate any more.

List of Posters in ITC 2023

Poster ID	Submission #	Title
PO.1	10	An Optimized Thermal Control Methodology for Burn-In and Qualification Stress on Automotive MCUs/MPUs
PO.2	11	BIST for Arm’s 3nm Multi-Port Register Files
PO.3	82	Correctness Checking for Neuromorphic Computing Systems
PO.4	130	Automatic Generation and Validation of System Verilog Assertions from Natural Language Specifications
PO.5	153	Deploying cutting-edge adaptive test analytics apps based on a closed-loop real-time edge analytics and control process flow into the test cell
PO.6	164	Transfer Learning in MCU Performance Screening
PO.7	165	Machine Learning Enhanced Kernel Based Cluster Fault Analysis
PO.8	166	Optimization of Scan VMIN Capability Grouping for Enhanced Defect Detection
PO.9	168	Automated Scan Chain Fault Isolation with Dynamic Voltage in Packetized Scan Network
PO.10	169	ITC-poster-abstract-Serdes Controller To PHY Loopback Test Method Sharing
PO.11	170	ITC-poster-abstract-DRAM DPM Reduction For 5G ASIC Product
PO.12	171	A Breakthrough Solution to Improve BISR Repair Data Visibility in HVM
PO.13	172	A Fast Turnaround SerDes GUI Debug Solution
PO.14	173	MBIST Test Time Reduction by Parallel Testing with Multi-TAP
PO.15	174	On-Chip Delay Measurement for Degradation Detection and Prediction
PO.16	175	Leveraging DeepLearning to Predict Memory Faults from Hardware Architectures
PO.17	176	Validation of Ultra-low Jitter-Reduction Techniques up to 20 GHz
PO.18	177	Power, Timing and Physically Aware Test points Exploration at RTL
PO.19	178	Scan Diagnosis On The Cloud

PO.20	179	ATE Integration of High Performance, High Data Rate 3rd Party Instruments for Reliable Manufacturing Test
PO.21	180	Scan Channel Configuration Selection using ML for Test Metric Prediction
PO.22	181	Inverse mapping Scan Diagnosis with Transformer Neural Networks
PO.23	182	Structural Tests over HSIO on SLT (ATS 7038)
PO.24	183	Teradyne’s PortBridge Expedites Complicated SOC Debug by Integrating Comprehensive Industry Tools
PO.25	184	General Purpose ATE Software
PO.26	185	Memory test automation using shared bus interface aids with turnaround time
PO.27	186	Automotive ASIC Test time reduction with Observation Scan Technology (OST)
PO.28	187	Effective Yield Boost and Cost Saving by Volume Diagnosis using Yield Explorer
PO.29	188	Cell-Aware Failure Analysis: Advanced Cell-Aware techniques to identify the FEOL/MOL layer systematic defects in cutting-edge technology
PO.30	189	Test Scalability with Sequential Compression Technology
PO.31	190	Test Robustness and Glitch Detection with TestMAX Advisor
PO.32	191	Advanced Test Point and Wrapping Techniques for Automotive Designs
PO.33	192	Physical Connection Aware SMS BIST Implementation for Abutted Design
PO.34	193	Holistic Approach to Solving Silent Data Corruption
PO.35	194	Deep Silicon Data and Analytics for Lifelong Safety and Reliability
PO.36	195	The Importance of Sensor Analytics in Enabling Silicon Lifecycle Management
PO.37	196	Dynamic Power Reduction for Hierarchical Test
PO.38	197	Extended Feature Testing using MBIST
PO.39	198	Pre-Silicon Estimation of Scan Chain Diagnosability
PO.40	199	Efficiency of packetized data delivery in 2.5D/3D designs
PO.41	200	Adaptive DFT technology in use with Automated Test Equipment (ATE)
PO.42	201	RTL DFT Analysis and Insertion of Test Points at RTL
PO.43	202	Clocking (DFT) considerations in designs with packetized scan data
PO.44	203	New TestMAX XLBIST Parallel Interface