TEST

INTERNATIONAL CONFERENCE

OCTOBER 8–13 2023

Disneyland Anaheim, CA

ITC Welcome Message

Welcome to our second hybrid ITC! We have a fantastic program that addresses new test technology challenges that significantly affect today's electronic products! In 2022 ITC attendees had a great time talking to each other in person. Time to renew your networking skills in 2023.

ITC is the world's premier conference dedicated to electronic test. This year's ITC continues with its mission to play a unique role as an **information sharing forum,** where the wide range of its offerings allows ITC participants to learn, network and conduct business. This year's program includes a top-notch technical program, vibrant exhibitors, information-packed **tutorials**, interactive technical **panels**, three focused **workshops**, as well as the all-important networking that these events can provide. The technical program has been designed to optimize personal interactions on all levels. This year's program will include papers from a pool of impressive submissions and solicited papers. See below for a list of sessions and papers.

ITC 2023 has a special focus on Diversity, Equity and Inclusion (DEI.) We are having a special panel on DEI, and some new DEI events. Stay tuned for more information.

In 2023 ITC will have three focus topics on our three days. They are Heterogeneous Integration (3DIC Day), Artificial Intelligence and Silicon Lifecyle Management. Look for paper tracks on these subjects in the program. We have two **keynotes** that will encompass the past, present and future of our industry. In addition, there will be a **visionary talk** on automotive test. New to ITC 2023 is a special Plenary Panel on the Metaverse.

ITC 2023 features a vibrant **exhibition** showcasing relevant companies. The exhibition will serve as a convenient one-stop shop for all the elements of test technology.

In the past 54 years, ITC has helped globalize our industry and wants to continue to do so in the future. This year's return to a live event will enable us to embrace all the features of the conference we have missed such as personal interaction and networking. Join us for the Wine and Cheese event after the Monday evening panel which kicks off ITC 2023. The ITC Grand Reception will be held Tuesday evening on the beautiful Adventure Lawn.

Last, but not least, we would like to recognize the enormous efforts of the multitude of dedicated volunteers who made ITC possible by donating their time, expertise, and enthusiasm. Without their hard work and dedication, ITC would not be possible. Please feel free to contact us if you would like to join our exciting team in the future.

ITC is the premier event for networking, where professionals from all over the world converge to sharpen skills, exchange ideas and do business. Join us, throughout the conference, for networking activities to unwind at the "Happiest Place on Earth", Disneyland!

Li-C Wang
General Chair

Jeff Rearick
Program Chair

Sponsors

IEEE

IEEE Philadelphia Section

IEEE COMPUTER SOCIETY

Corporate Supporters

Diamond

SIEMENS

Platinum

ADVANTEST SYNOPSYS Silicon to Software GALAXY TERADYNE

Gold

Chroma Advancing Excellence arm

Silver

cadence testinsight LINKING DESIGN & TEST

	Sunday	Monday	Tuesday	Wednesday	Thursday	Friday
12 Half-Day TTTC Tutorials A great way to prepare for the ITC Technical program	●	●				
Five Panels		●	●	●	●	
Plenary Sessions, 3 Keynotes, 1 Visionary Talk			●	●	●	
Over 45 Technical Presentations			●	●	●	
World-Class Exhibits			●	●	●	
36 Posters				●		
Two-Day Workshops Three to choose from					●	●

Become an ITC corporate supporter or utilize marketing opportunities

http://www.itctestweek.org

Follow Us On twitter

www.twitter.com/itctestweek

SUNDAY, OCTOBER 8 – HALF-DAY TUTORIALS			
8:30 a.m. – 12:00 p.m.	Tutorial 1 Dependability and Testability of AI Hardware	Tutorial 2 Early System Reliability Analysis for Cross-layer Soft Errors	Tutorial 3 Device-Aware Test for Emerging Memories. The Means to Win the War on Unmodeled Faults
1:00 p.m. – 4:30 p.m.	Tutorial 4 Random Process Variations, Circuit Timing Marchinalities and Silent Data Errors	Tutorial 5 Mixed-Signal DFT Challenges and Solutions	Tutorial 6 Hierarchical and Tile-Based DFT Techniques for AI and Large SOC

MONDAY, OCTOBER 9 – HALF-DAY TUTORIALS			
8:30 a.m. – 12:00 p.m.	Tutorial 7 Silicon Lifecycle Management for Emerging SOCs	Tutorial 8 Functional Safety Readiness Requirements in Design and Test Applications	Tutorial 9 Domain-Specific Machine Learning in Semiconductor Test
1:00 p.m. – 4:30 p.m.	Tutorial 10 Automotive Safety, Reliability and Test Solutions	Tutorial 11 Testing and Monitoring of Die-to-Die Interconnects in a 2.5D/3D IC	Tutorial 12 Functional Testing Techniques
4:30 p.m. – 6:00 p.m.	Panel 1- Grand Challenges in Test		

TUESDAY, OCTOBER 10 – TECHNICALSESSIONS				
9:00 a.m. – 10:30 a.m.	Plenary – **On-Package Chiplet Innovations with Universal Chiplet Interconnect Express (UCIe): Challenges and Opportunities** **Debendra Das Sharma, *Intel***			
10:30 a.m. – 5:30 p.m.	Exhibits			
10:30 a.m. – 10:45 a.m.	Coffee Break			
10:45 a.m. – 11:45 a.m.	Diamond Supporter Presentation			
11:45 a.m. – 1:30 p.m.	Lunch / Technical Women's Lunch, South Lounge			
1:30 p.m. – 3:00 p.m.	Session A1 Industrial Practices (Long Papers)	Session B1 Analog	Session C1 Test Technology Standard Committee (Special Session)	Session D1 Modern Memory Trends
3:00 p.m. – 4:00 p.m.	Coffee Break			
4:00 p.m. – 5:30p.m.	Session A2 Industrial Practices (Short Papers)	Session B2 Yield, Delay Test and More (Short Papers)	Session C2 Platinum Supporter Presentations	Session D2 HIR & UCIe (special session)
6:30 p.m. – 8:30 p.m.	ITC Welcome Reception			

WEDNESDAY, OCTOBER 11 – TECHNICAL SESSIONS				
8:30 a.m.–10:00 a.m.	Plenary Session **Delivering the Metaverse Vision with AI, AR/VR and Silicon Design Innovations**			
10:00 a.m. – 4:30 p.m.	Exhibits			
10:00 a.m. – 10:30 a.m.	Coffee Break			
10:30 a.m.–12:00 p.m.	Session A3 AI 1	Session B3 Emerging 1	Session C3 Metaverse (special session)	Session D3 TTTC PhD Competition
12:00 p.m.–2:00 p.m.	Lunch Poster Presentations .			
2:00 p.m.–2:40 p.m.	Visionary Talk Dipti Vachani. Four Wheels and A Billion Lines of Code – Enabling the Future of Automotive			
2:40 p.m.–3:30 p.m.	DEI Panel – Allyship in the Test Community			
3:30 p.m.–4:30p.m.	Coffee Break			
4:30 p.m.–6:00 p.m.	Session A4 AI 2	Session B4 Emerging 2	Session C4 AI Functional Safety	Session D4 Panel: AI in EDA and Test

Registration Hours

Sunday, October 8: 7:30 a.m. – 3:00 p.m.

Monday, October 9: 7:30 a.m. – 5:00 p.m.

Tuesday, October 10: 8:00 a.m. – 6:00 p.m.

Wednesday, October 11: 8:00 a.m. – 4:00 p.m.

Thursday, October 12: 8:00 a.m. – 3:00 p.m.

Friday, October 13: 7:30 a.m. – 12:00 p.m.

Registration is closed from 12:00 p.m. to 1:00 p.m. Tuesday to Thursday,

and 11:00 a.m. to 1:00 p.m. Sunday and Monday

THURSDAY, OCTOBER 12 – TECHNICAL SESSIONS				
9:00 a.m. – 10:00 a.m.	Plenary Session Keynote: TBA			
10:00 a.m. – 1:30 p.m.	Exhibits			
10:00 a.m. – 10:30 a.m.	Coffee Break			
10:30 a.m.–12:00 p.m.	Session A5 Automotive Test	Session B5 Post Silicon 1	Session C5 CHIPS Act Panel	Session D5 SLM In-field Testing
12:00 p.m. – 1:30 p.m.	Lunch			
1:30 p.m.–3:00 p.m.	Session A6 Security	Session B6 Post Silicon 2	Session C6 Panel: Will Silent Data Errors Give a New lease on Life to Semiconductor Test?	Session D6 ITC India

THURSDAY,OCTOBER 12– WORKSHOPS			
4:00 p.m. – 5:00 p.m.	ART 2023: IEEE Automotive Reliability and Test & Safety Workshop 2023	3rd IEEE Intl Workshop on Silicon Lifecycle Management (SLM)	IEEE TPTR: Top Picks in Test and Reliability

FRIDAY, OCTOBER 13 – WORKSHOPS			
9:00 a.m. – 4:00 p.m.	ART 2023: IEEE Automotive Reliability and Test & Safety Workshop 2023	3rd IEEE Intl Workshop on Silicon Lifecycle Management (SLM)	IEEE TPTR: Top Picks in Test and Reliability

All times are Pacific Daylight Savings Time

TTTC TEST TECHNOLOGY EDUCATION PROGRAM (TTEP) 2023

The Tutorials & Education Group of the IEEE Computer Society Test Technology Technical Council (TTTC) organizes a comprehensive set of Test Technology Tutorials to be held in conjunction with several TTTC-sponsored technical meetings worldwide. The mission of the Test Technology Educational Program (TTEP) is to serve test and design professionals by offering fundamental education and expert knowledge in state-of-the-art test technology topics. TTEP offers tutorial participants the opportunity to earn official certification from IEEE Computer Society TTTC. Each half-day tutorial corresponds to two TTEP units. Upon completion of 16 TTEP units, official recognition in the form of an IEEE TTTC Test Technology Certificate will be presented to the participant. For further information regarding TTEP, please visit http://ttep.tttc-events.org/ttep/index.html

At ITC 2023, TTTC/TTEP is pleased to present 12 **half-day tutorials** on topics of current interest to test professionals and researchers. All tutorials qualify for credit towards IEEE TTTC certification under the TTEP program. Six tutorials are held on Sunday, October 8. Six tutorials will be held on Monday, October 9.
The **one-day** tutorial registration fee is for two tutorials—a morning tutorial and afternoon tutorial, both on the same day, e.g., Tutorial 1 and Tutorial 4 on Sunday. You may register for up to four tutorials (two consecutive tutorials on Sunday and two consecutive tutorials on Monday).
The **all-access pass** tutorial registration provides in-and-out access to all twelve tutorials over both days.
(see registration page or http://www.itctestweek.org for further information).

Sunday 8:30 a.m. – 12:00 p.m. PDT

TUTORIAL 1
Magic Kingdom Ballroom 1
Dependability and Testability of AI Hardware

Presenters: F. Su, H. Stratigopoulos, Y. Makris

Toward continued performance improvement despite the slowed-down physical device scaling, adoption of bold and radical innovations in computer architectures has recently accelerated. One such trend focuses on computing architectures for AI hardware. While functionality of AI hardware still remains the main focus, testability and dependability of these new architectures need to be addressed before mainstream adoption. This tutorial covers the state-of-the-art in research and development of dependability and testability solutions for AI hardware (including digital or analog implementations of artificial neural networks (ANNs) and spiking neural networks (SNNs), used in accelerators and neuromorphic designs) and discusses challenges and future trends.

TUTORIAL 2
Magic Kingdom Ballroom 3
Early System Reliability Analysis for Cross-layer Soft Errors

Presenters: A. Bosio, S. Di Carlo, A. Salvino

In a world with computation at the epicenter of every activity, computing systems must be highly reliable even if miniaturization makes the underlying hardware unreliable. Techniques that guarantee high reliability are associated with high costs (reliability tax). Early reliability analysis can take informed design decisions to maximize reliability while minimizing the reliability tax. This tutorial focuses on early cross-layer reliability analysis considering the full computing continuum (from IoT/CPS to HPC applications), emphasizing soft errors. The tutorial will guide attendees from the definition of the problem down to the proper modeling and design exploration strategies considering the entire system stack.
.
.
.

TUTORIAL 3
Magic Kingdom Ballroom 4
Device-Aware Test for Emerging Memories: The Means to Win the War against Unmodeled Faults

Presenter: S. Hamdioui

This tutorial discusses a new test approach called Device-Aware Test (DAT) and applies it to two industrial memory designs: STT-MRAMs and RRAMs. DAT is a new test approach that goes beyond Cell-Aware Test; it does not assume that a defect in a device can be modeled electrically as a linear resistor (as the state-of-the art approach suggests), but it rather incorporates the impact of the physical defect into the technology parameters of the device and thereafter in its electrical parameters. Once the defective electrical model is defined, a systematic fault analysis is performed to derive appropriate fault models and subsequently test solutions. The tutorial discusses the testing of interconnect and contact defects as well as unique device defects in STT-MRAMs/ RRAMs. Unique defects are manufacturing defects are BEOL (back-end of line) defects that emerge due to the additional processing steps needed for the integrations of STT-MRAM/ RRAMs. Examples of STT-MRAM unique defects are pinhole and synthetic anti-ferrimagnet flip, and example of RRAM unique defects are forming and ion depletion defects. Industrial case studies for STTMRAM and RRAM show that DAT sensitizes realistic faults as well as new unique defects and faults that can never be caught with the traditional approaches.

Sunday 1:00 p.m. – 4:30 p.m. PDT

TUTORIAL 4
Magic Kingdom Ballroom 1
Random Process Variations, Circuit Timing Marginalities and Silent Data Errors

Presenter: A. Singh

Computation-in-Memory New types of failures that escape traditional scan DFT tests are being increasingly observed in SOCs. For example, recent presentations (since 2021) from Google and Facebook (Meta) have reported significant levels of silent data corruption in their large data centers. These occasional transient failures have been associated with specific processor cores in these large processor networks, suggesting faulty or unstable hardware from test escapes rather than failures from random environmental noise. The inability of scan structural tests to detect these failures has resulted in the introduction of an entirely new function system level test (SLT) over the past few years, to serve as an additional final defect screen in manufacturing test flows. However, even these expensive functional tests allow significant test escapes that cause malfunction in operation. We explain why timing marginalities resulting from manufacturing process variations, greatly accentuated in low voltage operation, are the likely cause of much of the SLT fallout. Furthermore, these failures can even escape detection by SLT and can cause many of the silent data errors reported by datacenters. To explain this, we review scan DFT tests in depth, including recent advances such as cell aware test, path delay tests, and timing aware tests. This helps us understand why scan tests are unable to reliably detect timing errors from process variations. Finally, we present and explain research, as validated on published volume production test data from Intel'™s advanced 14nm FinFET technology, which suggests ways of leveraging the voltage and timing of the applied timing tests to enhance the detection of marginal timing parts during scan and system level testing. The goal is to reliably screen out these marginal parts during postproduction testing and thereby prevent them from causing errors in operation..

TUTORIAL 5
Magic Kingdom Ballroom 3
Mixed-Signal DFT Challenges and Solutions

Presenter S. Sunter

This tutorial explores systematic analog and mixed-signal design-for-test, including analog fault/defect simulation. We review widely-used basic DfT techniques, fault simulation, IEEE 1149.1/4/6/7, 1687, and ISO 26262 metrics, then BIST for ADC/DAC, PLL, SerDes/DDR, and random analog. Essential principles of practical analog BIST are presented, then practical DfT techniques, from quicker analog defect simulation to DfT that focuses on simplicity, diagnosis, reuse, and automation. We conclude with a detailed summary of the Analog Defect Coverage and Analog Test Access standards (IEEE P1687.2, P2427), as they approach completion thanks to the effort of dozens of people over many years..

TUTORIAL 6
Magic Kingdom Ballroom 4
Hierarchical and Tile-Based DFT Techniques for AI and Large SOC

Presenters: L. Harrison, P. Orlando

In this tutorial, we will proceed to give an overview of the exciting field of AI and HPC. It will cover the critical and special characteristics and the architecture of the popular AI chips. Next we will summarize the features of the AI chips from design-for-test (DFT) perspective and introduce the DFT technologies that can help testing AI chips. We will also look at how the shift to 2.5D and 3D including Chiplet development is changing the industry and the adding new challenges for the DFT community Finally, we will present a few case studies on how DFT is implemented in the real AI chips. We will also present some of the functional monitoring techniques that are available today. An overall architecture showing how functional monitoring can be implemented and how the monitor data can be used to manage in-life capabilities. Finally, we will present a few case studies on how DFT is implemented in the real AI chips.

.

Monday 8:30 a.m. – 12:00 p.m. PDT

TUTORIAL 7
Magic Kingdom Ballroom 1
Silicon Lifecycle Management for Emerging SOCs

Presenter: Y. Zorian

Recent advances in automotive SOCs, artificial intelligence accelerators, and high-performance computing engines in data centers have led to an explosion in the adoption of emerging technology nodes and 3DIC/chiplet packages. This tutorial will present todayâ€™s trends and discuss the resiliency challenges for such emerging SOCs. It will focus on optimizing the SOC health using advanced test, measurement and analytic solutions, such as on chip structural sensors, functional monitors, environmental sensors and embedded test & repair engines, typically utilized for managing the different silicon lifecycle stages: from silicon debug in early bring up stage to shorten the time-to-volume; to self-test and repair during volume production stage, in order to improve quality and yield; to power-on self-test in the field stage to address aging challenges; to periodic checking in-system to improve functional safety; and finally to fault tolerance and error correction during mission mode to address a range of transient errors. All of the above optimizations are materialized by on-chip and/or off-chip data analytics.
.

TUTORIAL 8
Magic Kingdom Ballroom 3
Functional Safety Readiness: Requirements in Design, Test, and Application

Presenters: R. Parekhji, P. Viswanathan Pillai

This tutorial covers, (and in the process demystifies), four aspects of semiconductor functional safety: (a) How are the well-known metrics for ASIL (automotive) and SIL (industrial) classification set. (b) How do these requirements drive the selection of the right set of detection and diagnostics mechanisms. (c) How is conformance to these classification levels assessed. (d) How are fault spaces and coverage numbers apportioned to different IC building blocks and higher level compositions at the system level. Industry examples highlighting how these requirements in design, test and application can drive readiness for functional safety will be discussed..

TUTORIAL 9
Magic Kingdom Ballroom 4
Domain-Specific Machine Learning in Semiconductor Test

Presenter: L-C. Wang

The emerge of large Language Model (LM) have significantly impacted our view for applying Machine Learning (ML) in semiconductor test. Recent LMs include Codex focusing on code generation and InstructGPT for capturing user intent. Their successor, ChatGPT, has demonstrated remarkable performance for engaging in dialog on a wide variety of topics, answering questions, and generating code. With these recent LM technological developments, this tutorial provides an integrated view of Domain-Specific Machine Learning (DSML) in semiconductor test. This view calls for an end-to-end AI solution to realize DSML. In our domain, DSML is applied in an iterative exploration process for an engineer to learning knowledge from data. In this iterative process, ML is applied to facilitate an engineer to move from one iteration to the next. To illustrate this DSML view, we will discuss common test data analytics practices including outlier analysis, wafer map pattern recognition, yield optimization, and cross-insertion predictive analysis, and explains their challenges and current solutions. We will then discuss the latest LM technologies and how they fit into our DSML view to build an end-to-end AI solution. Industrial case studies will be provided to illustrate the concepts taught in this tutorial.

Monday 1:00 p.m. – 4:30 p.m. PDT

TUTORIAL 10
Magic Kingdom Ballroom 1
Automotive Safety, Reliability and Test Solutions

Presenters: R. Mariani, Y. Zorian

With the fast-growing adoption of advanced technology nodes for automotive chips, this tutorial will discuss the implications of automotive quality, functional safety, and reliability on all aspects of automotive SOC lifecycle, while accelerating time to market for these semiconductor ICs. The automotive SOC lifecycle stages will include design, silicon bring-up, volume production, and particularly in-system operation. Today's automotive safety critical chips need multiple in-system modes, such as power-on and power-off self-test and repair (key-on/key-off), periodic in-field self-test during mission mode, advanced error correction solutions, etc. This tutorial will analyze these specific in-system test modes and discuss the benefits of using ISO 26262 including its second edition, and several newer standardization efforts, to ensure that standardized functional safety requirements are met.

TUTORIAL 11
Magic Kingdom Ballroom 3
Testing and Monitoring of Die-to-Die Interconnects in a 2.5D/3D IC

Presenter: S-Y Huang

With the evolution of multi-die integration into the era of interposer- or InFO-based 2.5-D ICs and/or TSV-based 3D stacked ICs, die-to-die interconnects could operate in a very high speed, with an end-to-end delay of only a few hundreds of picoseconds. Parametric defects (like small delay faults, resistive open/bridging faults, leakage faults, etc.) have been identified as potential threats to the yield and reliability of a 2.5D/3D IC product. Fortunately, various test and online monitoring methods have been developed to deal with this challenge and to guarantee the overall quality of the die-to-die interconnects in a 2.5D/3D IC product..
.

TUTORIAL 12
Magic Kingdom Ballroom 4
Functional Testing Techniques

Presenter P. Bernardi

Since the inception of IC design in the mid-1960s, IC test has been an integral part of the manufacturing process. Initially, tests were of the Functional nature of either randomly generated or created from verification suites. But as chips got larger, testing required a more targeted approach, one that needed to be easily replicated from one design to another. This led to the invention of Structural methods like scan, which made designs combinational and simplified the test generation process. After almost 50 years, the testing scenario evolved just slightly, following technology trends currently led by the complexity of the circuits under test and the field of use (i.e., Automotive). Structural methods are still dominant, at least during the manufacturing test process, but Functional techniques are now recognized to be: (i) Useful to complement structural techniques during the manufacturing test process, such as System Level Test. (ii) Able to mitigate thermal issues that may originate during stress phases like along Burn-In, thus enabling test data collection during this phase. (iii) Very helpful along with the useful life of the components in the mission field, to run a not destructive self-test and also able to capture and store information, opening possibilities for Silicon Lifetime Management (SLM). The talk will provide basic and practical information about some today-relevant functional techniques in the field of Software-Based Self-Test (SBST), Burn-In Functional Stress/Test (TDBI), and System-Level Test (SLT). Automotive chip case studies from STMicroelectronics will be illustrated.

Click on an Exhibitor Name to go to their Website

Featured Exhibitors

Chroma ATE Booth # 117

Chroma ATE Inc. is a world-leading designer and manufacturer of complete turnkey , IC thermal management and automated IC Handling solutions. Specializing in integrated and fully automated turn-key electronic test and MES solutions for the semiconductor, front and back-end test spaces. Chroma is driven to provide unique, tailored solutions, and technical support to help our US-based customers excel in today's high demanding environment.

Siemens Booth # 205

Siemens is the technology and market leading provider of design-for-test solutions. With the industry's only comprehensive hierarchical DFT offering, our solutions enable our customers to achieve the lowest cost of test, highest test quality, fastest yield ramps and meet the most rigorous functional safety requirements demanded by the automotive market's ISO 26262 standard.

Synopsys, Inc Booth # 105

The Synopsys TestMAX™ family offers unparalleled test quality and efficiency, with tight integration across the Synopsys Fusion Design Platform to enable faster turnaround time while uniquely meeting both design and test goals concurrently.

Regular Exhibitors

Advantest Booth # 217

Advantest is the leading manufacturer of automatic test and measurement equipment used in the design and production of semiconductors for applications including 5G, IoT, autonomous vehicles, high-performance computing (HPC), including AI and machine learning, and more. Its leading-edge products are integrated into the most advanced semiconductor production lines in the world. The company also conducts R&D to address emerging testing challenges and applications; develops advanced test-interface solutions for wafer sort and final test; produces scanning electron microscopes essential to photomask manufacturing; and offers system-level test solutions and other test-related accessories. Founded in Tokyo in 1954, Advantest is a global company with facilities around the world and a commitment to sustainable practices and social responsibility. Learn more at www.advantest.com.

** As of publication date*

Dynamic Test Solutions Booth # 222

Dynamic Test Solutions (DTS) was founded in 2003. The company is structured to support the engineering, Si / Pi simulations, design, fabrication and assembly of custom and generic PCBs for wafer and package test applications for a complete turnkey ATE hardware solutions. DTS has built its reputation on providing outstanding customer service. Taking that service and support directly to the customer in locations throughout the world is what differentiates DTS from the competition. DTS has built a global organization that includes sales, customer service, applications engineering, Si / Pi simulations, design centers, PCBs fabrication, assembly and Quality Assurance in all key geographic regions. www.dynamic-test.com

Eles Semiconductor Booth # 309

Exatron Booth # 318

Exatron is a full-service automation provider, founded in 1974, based in California. We design and build pick-n-place, rotary, tape-n-reel, & gravity feed into test, vision, laser, temperature, & MEMS applications.

Ironwood Electronics Booth # 111

Includes 75 GHz bandwidth sockets for BGA and QFN, only slightly larger than IC with integral heatsink for medium power and optional heatsinking to over 100 watts. Up to 500k insertions. Adapters for prototype, test, package conversion, and more. Quick-Turn volume adapters are our specialty.

Micro Control Company Booth # 210

Micro Control Company is the test with burn-in expert. Devices that successfully complete a burn-in cycle in a Micro Control burn-in with test system are proving significantly more reliable for long-term use. Micro Control Company's burn-in systems increase device reliability by applying electronic stimulation to the devices under test during the burn-in cycle. Stressing the devices during burn-in causes devices that are going to fail, to fail early. By monitoring the devices as they are being stressed, the failing devices are detected and eliminated from the lot.

National Instruments Booth # 223

Discover the latest NI solutions to enable data-driven capabilities for automation and standardization to address the challenges of increased product complexity, time-to-market demands, and manufacturing volumes. Visit us at booth #223!

NHK Spring Co. Booth # 123

Roos Instruments Booth # 316

Roos Instruments is the premier supplier of highly automated test solutions for wireless devices. Our system's perfo mance and technical expertise are the tools our customers rely on to meet the challenges of next generation products.

Salland Engineering Booth # 200

Salland Engineering in Zwolle – The Netherlands is an international leading Test Technology & Engineering company specialized in solutions and services that enable semiconductor manufacturers to improve the efficiency and quality of their testing. Our Solutions are delivered via a unique combination of innovative Test Technology and realization including Instruments, Applications expertise and supply chain & test services.

TDK-Lambda Americas Booth # 323

TDK-Lambda Americas, Inc. is a leading manufacturer of high reliability Low/High Voltage Programmable DC and High Voltage Programmable Capacitor Charging power supplies and DC Electronic Loads. Programmable DC products include the Genesys™Series, the GENESYS+™ Series, the ALE Series and the SFL Series. For more information, please visit https://www.us.lambda.tdk.com.

TESEC Booth # 311

Tesec is a world leader in power semiconductor test and automation. We provide high-volume production and engineering test solutions for a variety of applications including High-Power & High-Reliability devices, MEMS, and WLCSP/Strip-Test.

Test Spectrum Booth

Test Spectrum is a recognized leader in semiconductor test solutions. We provide software products that are essential tools for every test engineer and world class engineering services in test software and test hardware development.

Our customers include fabless semiconductor companies, integrated device manufacturers (IDMs), automated test equipment companies (ATE), test and assembly houses, and IP companies from across the globe.

Founded in 1999 in Austin, Texas, Test Spectrum is committed to excellence in semiconductor test solutions through experience, execution, and integrity.

TSE Booth # 319

TSE is a company specializing in semiconductor inspection equipment. Among the inspection equipment used in the wafer test and package test process, typical consumable and model replaceable products include probe card, package test interface board (TIB), and test socket. TSE is the only company in the world that manufactures & supplies all three products. The core competitiveness is that we have a business structure that creates mutual synergy with representative semiconductor inspection devices such as probe card, TIB, and test socket technology, and that it has good internalization and vertical integration of major parts. Through this, we can achieve the business structure that facilitates the development of turnkey solutions and convergence products.

TSSI Booth # 315

Founded in 1979, TSSI is a worldwide leader in design-to-test conversion and validation software solutions. Our all-in-one graphical user interface allows all tools available at your fingertips, and data to be visualized throughout the vector translation process. Vector translation should not be a blind-conversion where extra steps are needed to even know whether the output patterns are correct. Also come to see how TSSI VirtualTester reduces silicon bring-up time from months to hours, and how 100% test patterns worked the first time. If visiting our physical booth in-person at Disneyland Hotel, come by to get a chance to win an Apple product!

TTTC Booth # 201

TTTC's goals are to contribute to our members' professional development and advancement, to help them solve engineering problems in electronic test, and to help advance the state-of-the art.

yieldHUB Booth # 305

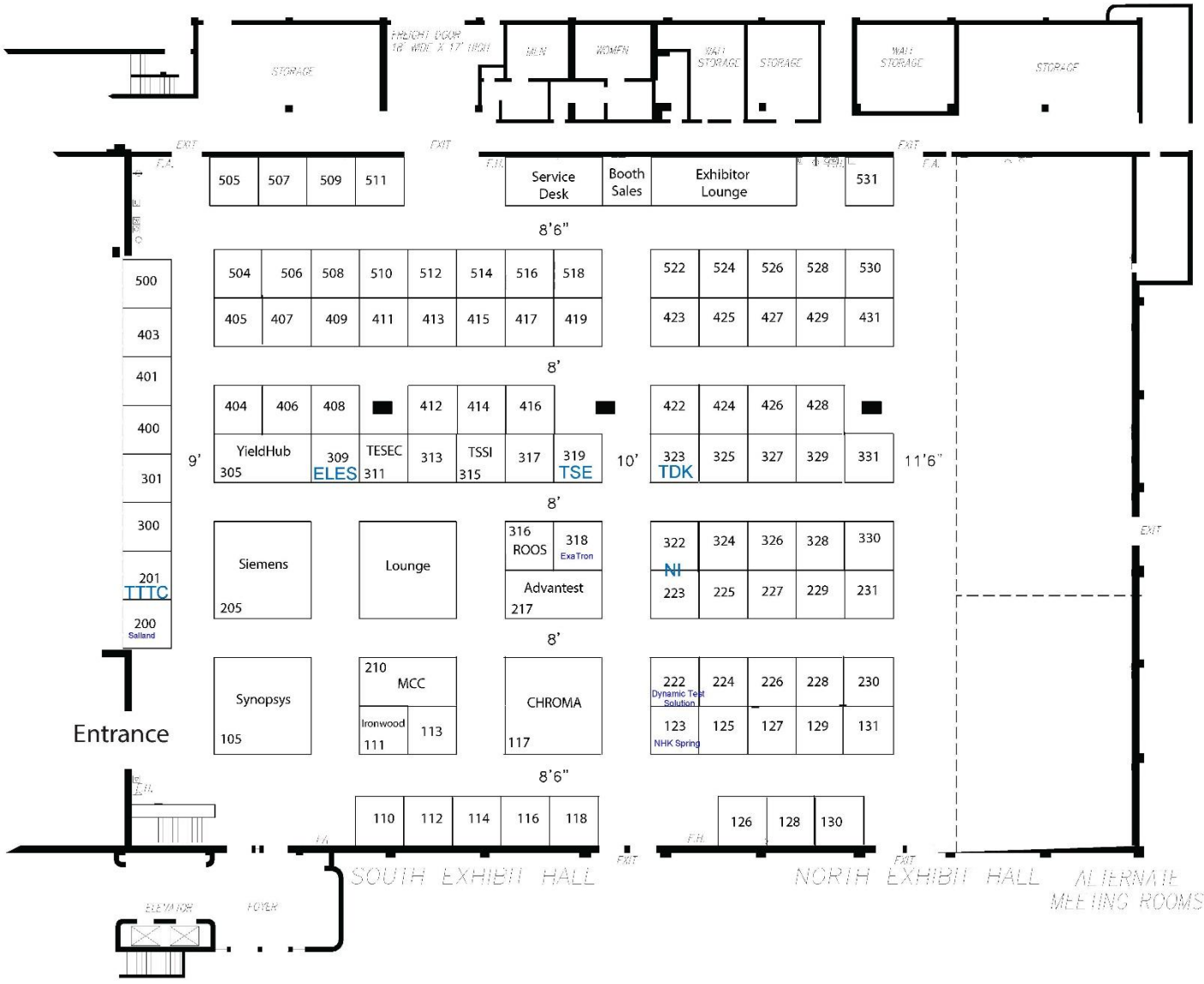
With today's added pressures of time to market, along with the high cost of manufacturing, and material shortages, it's never been a better time for semiconductor companies and fabless startups to invest in a yield management platform. yieldHUB was designed to offer modern automated solutions for all yield management challenges.

Smart engineering is at the core of our platform, which was built so engineers can easily access and analyze data with unrivaled speed and accuracy. As volume grows, yieldHUB users can analyze and stack hundreds and even thousands of wafers at the same time using our cloud product on a web browser. Your engineers will be able to monitor production from any device no matter where they are.

The yieldHUB platform offers exclusive and unique features to its customers, combined with intuitive design, innovative communication tools, and help from our team of highly experienced experts. We've helped improve the yield for manufacturers of 60 billion chips in the past year.

You could be just a few clicks away from having all of your yield management problems solved by our team today. Visit *www.yieldhub.com* to get started.

INTERNATIONAL TEST CONFERENCE
October 2023
Disneyland Hotel Convention Center



ITC 2023 Supporter Information

ADVANTEST®

Visit Booth# 223 to Learn about Latest Test Technologies

TERADYNE

Creating the Next Generation of Technology Through Advanced Test Solutions

TERADYNE.COM

Tuesday 9:00 a.m. – 10:30 a.m.

Opening Remarks
Li-C Wang, *ITC 2023 General Chair*

ITC 2023 Program Introduction
Jeff Rearick, *ITC 2023 Program Chair*

ITC 2022 Paper Awards Presentation
KJ Lee, *ITC 2022 Program Chair*

TTTC Awards Presentation
Yervant Zorian

Keynote Address

On-Package Chiplet Innovations with Universal Chiplet Interconnect Express (UCIe): Challenges and Opportunities

Debendra Das Sharma

Senior Fellow & co-GM, Intel

Abstract: High-performance workloads demand on-package integration of heterogeneous processing units, on-package memory, and communication infrastructure such as co-packaged optics to meet the demands of the supercomputing landscape. On-package interconnects are a critical component to deliver the power-efficient performance with the right feature set in this evolving landscape.
Universal Chiplet Interconnect Express (UCIe), is an open industry standard with a fully specified stack that comprehends plug-and-play interoperability of chiplets on a package; like the seamless interoperability on board with well-established and successful off-package interconnect standards such PCI Express® and Compute Express Link (CXL)®. In this talk, we will discuss the usages and key metrics associated with different technology choices in UCIe and how it will evolve going forward. We will also delve into the challenges and opportunities for chiplets connected through UCIe, including test and debug.
.
.

About the speaker:
Dr. Debendra Das Sharma is an Intel Senior Fellow and co-GM of Memory and I/O Technologies in the Data Platforms and Artificial Intelligence Group at Intel Corporation. He is a leading expert on I/O subsystem and interface architecture.
Dr. Das Sharma is a member of the Board of Directors for the PCI Special Interest Group (PCI-SIG) and a lead contributor to PCIe specifications since its inception. He is a co-inventor and founding member of the CXL consortium and co-leads the CXL Board Technical Task Force. He co-invented the chiplet interconnect standard UCIe and is the chair of the UCIe consortium.

Dr. Das Sharma has a bachelor's in technology (with honors) degree in Computer Science and Engineering from the Indian Institute of Technology, Kharagpur and a Ph.D. in Computer Engineering from the University of Massachusetts, Amherst. He holds 175 US patents and 450+ patents world-wide. He is a frequent keynote speaker, plenary speaker, distinguished lecturer, invited speaker, and panelist at the IEEE Hot Interconnects, IEEE Cool Chips, IEEE 3DIC, SNIA SDC, PCI-SIG Developers Conference, CXL consortium, Open Server Summit, Open Fabrics Alliance, Flash Memory Summit, Intel Innovation, various Universities (CMU, Texas A&M, Georgia Tech, UIUC, UC Irvine), and Intel Developer Forum. He has been awarded the Distinguished Alumnus Award from Indian Institute of Technology, Kharagpur in 2019, the IEEE Region 6 Outstanding Engineer Award in 2021, the first PCI-SIG Lifetime Contribution Award in 2022, and the IEEE Circuits and Systems Industrial Pioneer Award in 2022.

.
.

8:30 a.m. – 10:00 a.m.

Plenary 2: *J. Rearick* (Chair)

Delivering the Metaverse Vision with AI, AR/VR and Silicon Design Innovations
Organizer: Savita Banerjee, *Meta*
Moderator:
Speakers:

- Savita Banerjee, Sr. Manager DFx, *Meta*
- Caitlin Kalinowski, Head, AR Hardware, *Meta*
- Manohar Paluri, Senior Director, Generative AI, Meta

Hear thought leaders from Meta discuss how the Metaverse is expected to transform social connection as well as the challenges fueling a new wave of innovation and disruptive technology.

Speakers:

Savita Banerjee leads DFX strategy for Augmented Reality products at Meta's Reality Labs. She received her Ph.D. from the University of Massachusetts at Amherst and started her career at Bell Labs. Savita is recognized for her contributions to advancements in silicon technology for storage, networking, data centers and AR/VR applications. At Meta, she leads design for test strategy for the AR roadmap utilizing advanced process nodes with optimized flows to meet stringent product requirements. She is passionate about building disruptive technologies for next generation compute platforms that improve how we work, connect, and have fun.

Caitlin Kalinowski leads the AR Hardware team for Reality Labs at Meta. For the past seven years, she led VR Hardware, the division responsible for the Meta Quest 2 and Touch controllers, as well as the Oculus Rift. Before working at Oculus, Caitlin was a technical lead at Apple on the Mac Pro and MacBook Air products and was part of the original unibody MacBook Pro teams. Caitlin received her BS in Mechanical Engineering from Stanford University in 2007.

Manohar Paluri is a senior director at Meta and leads an organization focusing on Generative Artificial Intelligence. His team is at the intersection of research and product and powers image and video understanding capabilities for hundreds of products across all of Meta's family of apps serving Billions of people everyday.

9:00 a.m. – 10:00 a.m.

Plenary 3:

Title: TBA

Scott Runner
CEO, Cariad Inc.

Abstract: TBA

About the Speaker: Scott Runner has more than 30 years of software, hardware, and semiconductor experience in the global automotive and mobile communications industries. He also has extensive leadership experience in digital and cultural transformation. Runner began his career in 1985 at Fujitsu with subsequent positions at Synopsys, Conexant, and a start-up company consulting to ARM Ltd. In 2003, Runner joined Qualcomm to help build the US and India teams and methods that delivered the first and subsequent integrated smartphone SoCs. In 2012, Runner helped found the team that delivered Qualcomm's first two generations of automotive-grade infotainment and telematics products. Subsequently, Runner joined what became Capgemini Engineering as the Global Practice Leader for embedded software, EE, and semiconductors responsible for consulting, solutioning, developing, validating, and testing of in-vehicle infotainment, ADAS/AD and telematics products and systems for OEM and tier1 clients. Scott is currently the CEO for CARIAD, Inc., where he leads a team focusing on hardware development, cloud technologies, and connected infotainment for Volkswagen Group Brands. He has a B.S. in applied physics and did graduate work in computer science and engineering management.

Wednesday, October 11
2:00 p.m. – 2:40 p.m.

Visionary Talk 1: *J. Rearick* (Chair)

Four Wheels and A Billion Lines of Code – Enabling the Future of Automotive

Dipti Vachani *Sr VP & GM, Automotive Business, ARM*

Abstraxtr We will give an overview of the objectives and some recent progress in designing ultra-low-power AI accelerators for supporting a wide range automotive industry is undergoing one of the most significant technology revolutions in human history, unleashed by the power of software. Vehicles of the future hold the potential to save millions of lives, help save the planet, and deliver enriching experiences that improve our quality of life. As future generations of vehicles adopt modern technologies and a rapid rise in electronics, we must work together as an industry to enable this critical transformation.

In her keynote, Dipti will discuss the holistic approach required to deliver these vehicles of the future and the investments required in hardware, software, and industry collaborations to make this vision a reality.

About the Speaker: Dipti leads the organization responsible for delivering Arm-based solutions in the transformational opportunities of automotive.
Previously, Dipti served as Vice President and General Manager of the Product Management and Customer Enablement division in the IoT Group at Intel. Before that, Dipti held several leadership positions at Texas Instruments and led the creation of the company's Sitara brand of Arm MPUs.

Dipti is on the Women's Leadership Council for the Global Semiconductor Association. She holds a BS in Computer Engineering from Texas A&M, an Executive MBA degree from the University of Texas, and is a graduate of the Executive Education programs at Stanford, Harvard, and Cambridge business schools.

*: Paper presenter

1:30 p.m. – 3:00 p.m. PDT

SESSION A1
Industrial Practices (Long Papers)
Magic Kingdom Ballroom 1
H. M. von Staudt, Renasas (Chair)

A1.1 A New Framework for RTL Test Points Insertion Facilitating a "Shift-Left DFT" Strategy
H. Iwata, Y. Maeda, J. Matsushima, DFT Platform Technology Section, Digital Design Technology Department; * *O. Laouamri, N. Khanna, J. Mayer, N. Mukherjee*, Silicon Lifecycle Solutions, Siemens Digital Industries Software

A1.2 A Case Study on IEEE 1838 Compliant Multi-Die 3DIC DFT Implementation
* *A. Chandra, M. Khan, S. Goel, A. Patidar, F. Takashima*, TSMC; *M. Arora, B. Shankaranarayanan, V. Tyagi, V. Nguyen*, Synopsys

A1.3 New Algorithm for Fast and Accurate Linearity Testing of High-Resolution SAR ADCs
* *A. R*, Texas Instruments

SESSION B1
Analog
Magic Kingdom Ballroom 2
(Chair)

B1.1 Improving Angle Of Arrival Estimation Accuracy for mm-Wave Radars
* *F. Ataman, S. Ozev*, Arizona State University; *C. Kumar Y.B.*, Texas Instrumentsx

B1.2 OATT: Outlier Oriented Alternative Testing and Post-Manufacture Tuning of Mixed-Signal/RF Circuits and Systems
* *S. Komarraju, A. Tammana, C. Amarnath, A. Chatterjee*, Georgia Institute of Technology

B1.3 Low Distortion Sinusoidal Signal Generator with Harmonics Cancellation Using Two Types of Digital Predistortion
* *K. Sato, T. Ishida, T. Okamoto, T. Ichikawa*, ROHM Semiconductor; *T. Nakatani, S. Katayama, D. Iimori, M. Takagi, A. Kuwana, K. Katoh, K. Hatayama, H. Kobayashi*, Gunma University; *Y. Zhao*, Division of Electronics and Informatics, Faculty of Science and Technology; *S. Yamamoto*, Division of Electronics and Informatics, Faculty of Science and Technology

SESSION C1
Test Technology Standards Committee (Special Session)
J. Rearick, AMD (Commentary)
Magic Kingdom Ballroom 3
Speakers:
1149.1 *H. Ehrenberg*, GoepelUSA
1687 *M. Keim*, Siemens
P2427 *A. Coyette*, On Semi
P1687.2 *S. Sunter*, Siemens
P1687.1, P2654 *J. Rearick*, AMD
P2929 *S. Menon*, Intel

SESSION D1
Modern Memory Trends (Special Session)
G. Harutyunyan, Synopsys (Commentary)

D1.1 Test Challenges for GAA in the Race Between Nanometers and Angstroms
K. Amirkhanyan, H. Danoyan, A. Ghukasyan, G. Harutyunyan, K. Kyuregyan, G. Tshagharyan, Synopsys, Armenia

D1.2: NN-ECC: Embedding Error Correction Codes in Neural Networks using Multi-task Learning
S. Tuhin, S. Hemaram, M. B Tahoori, Karlsruhe Institute of Technology, Germany

D1.3: DFT, Test Challenges and Solution to Enable the Large Scale SoC with HBM
S. Ikeda, H. Nishiwak Socionext; *A. Kumar*, Synopsys

4:00 p.m. – 6:00 p.m.

SESSION A2
Industrial Practices (Short Papers)
Magic Kingdom Ballroom 1
S. Ramesh, NXP (Chair)

A2.1 Maximizing Stress Coverage by Novel DFT Techniques and Relaxed Timing Closure
* *A. Sinha, G. Colon-Bonet, M. Fahy, P. Pant, H. Mao, A. Shukla*, Intel

A2.2 Novel Methodology to Optimize TAT and Resource utilization for ATPG Simulations for Large SoCs
S. Kongala, * *A. Gupta, Y. Walia, S. Jain*, Cadence Design Systems

A2.3 Global Control Signal Defect Diagnosis in Volume Production Environment
S. Urban, * *P. Zimnowlodzki, M. Sharma*, Siemens DISW; *S. Bodhe, , J. Schulze, A. Yassine, A. Styblinski*, Advanced Micro Devices, Inc.

A2.4 Method for Diagnosing Channel Damage using FPGA Transceiver
* *S. Lee, J. Won, C. Park, J. Choi, M. Kang*, Samsung Electronics

A2.5 Method for Adjusting Termination Resistor Value using PMU of ATE
* *S. Lee, M. Kang, C. Park, J. Choi, J. Won*, Samsung Electronics

A2.6 Transitioning eMRAM from Pilot Project to Volume Production
* *C. Dray*, Arm Sophia Antipolis, France; *K. Gelda*, Arm Bengaluru, Karnataka; *B. Nadeau-Dostie*, Siemens Ottawa, Canada;*W. Zou*, Siemens Wilsonville, USA; *L. Romain*, Siemens Ottawa, Canada;*J. Yun*, Siemens Wilsonville, USA; *H. Kodali*, Siemens Wilsonville, USA; *L. Schramm*, Siemens Atlanta, USA; *M. Keim*, Siemens Orlando, USA

SESSION B2
Yield, Delay Test and More (Short Papers)
Magic Kingdom Ballroom 2
H. Walker, Texas A&M University (Chair)

B2.1 Algorithmic Read Resistance Trim for Improving Yield and Reducing Test Time in MRAM
* *D. Chang, Y. Kim, S. Hun*, Samsung Electronics(Samsung Foundry)

B2.2 Machine-Learning Driven Sensor Data Analytics for Yield Enhancement of Wafer Probing
* *N. Sinhabahu, J. Wang, M. Ho*, NXP Semiconductors Taiwan Ltd.; *K-M. Li*, Dept. of Computer Science and Engineering; *S-J. Wang*, National Chung Hsing University

B2.3 Domain-Specific Machine Learning based Minimum Operating Voltage Prediction using On-Chip Monitor Data
* *Y. Yin*, University of California, Santa Barbara; *R. Chen, C. He*, NXP Semiconductors; *P. Li*, University of California, Santa Barbara

B2.4 Compaction of Functional Broadside Tests for Path Delay Faults using Clusters of Propagation Lines
* *I. Pomeranz*, Purdue University

B2.5 Robust Pattern Generation for Small Delay Faults under Process Variations
* *H. Jafarzadeh, F. Klemme, Z. Najafi Haghi, H. Amrouch, H-J. Wunderlich*, University of Stuttgart; *J. Reimer, S. Hellebrand*, University of Paderborn

B2.6 Logic Test Vehicles for High Resolution Diagnosis of Systematic FEOL/MEOL Yield Detractors
* *Y. Lyu, L. Yu, J. Huang,* HiSilicon Technologies Co, Ltd.; *P. Li*, University of California, Santa Barbara

SESSION C2
Presentations of Platinum Supporters
Magic Kingdom Ballroom 3
C-H Chiang, Intel (Chair)

SESSION D2
UCIe: Democratizing 3DIC and Chiplets Ecosystem (Special Session)
Magic Kingdom Ballroom 4
Y. Zorian (Commentary)
Presenters:
M. Braun, Advantest
D. Sharma, Intel
S. Goel, TSMC
Y. Zorian, Synopsys

*: Paper presenter

10:30 a.m. – 12:00 p.m. Pacific Daylight Time

SESSION A3
AI 1
Magic Kingdom Ballroom 1
J. Dworak, Southern Methodist Univ. (Chair)

A3.1 IEA-Plot: Conducting Wafer-Based Data Analytics Through Chat
*M. Dupree, M. Yang, * Y. Zeng, L-C. Wang,* UCSB

A3.2 Improving Efficiency and Robustness of Gaussian Process Based Outlier Detection via Ensemble Learning
** M. Eiki,* Sony Semiconductor Manufacturing; *T. Nakamura, M. Kajiyama,* Sony Semiconductor Manufacturing Corporation; *M. Inoue,* Nara Institute of Science and Technology; *T. Sato,* Kyoto University; *M. Shintani,* Kyoto Institute of Technology

A3.3 Recognizing Wafer Map Patterns using Semi-Supervised Contrastive Learning with Optimized Latent Representation Learning and Data Augmentation
** Z. Wang, H. Hu,* Electrical and Computer Engineering Department, University of California; *C. He,* NXP Semiconductors; *P. Li,* University of California, Santa Barbara

SESSION B3
Emerging 1
Magic Kingdom Ballroom 2
P. Wohl, Synopsys (Chair)

B3.1 Wafer-Scale Electrical Characterization of Silicon Quantum Dots from Room to Low Temperatures
** F. Lorenzelli, A. Elsayed, C. Godfrin, A. Grill, S. Kubicek, R. Li, M. Stucchi, D. Wan, K. De Greve, E. Marinissen,* IMEC; *G. Gielen,* KU Leuven

B3.2 GPU-based Concurrent Static Learning
** H. Liang, L. Lai,* Shantou University; *X. Lin,* Shantou University; Pengcheng Lab; University of Chinese Academy of Sciences; *N. Wang, Y. Huang, F. Yang, Y. Yang,* Huawei Hisilicon

B3.3 Biochip-PUF: Physically Unclonable Functions for Microfluidic Biochips
** N. Baban,* Center for Cyber Security, Department of Engineering; *U. Chatterjee,* Department of Computer Science and Engineering, Indian Institute of Technology Kanpur; *S. Bose,* Department of Chemical Engineering, Indian Institute of Technology Kharagpur; *A. Orozaliev,* Department of Engineering, New York University Abu Dhabi; *S. Bhattacharjee,* Department of Computer Science and Engineering, Indian Institute of Technology Guwahati; *Y-A. Song,* Center for Cyber Security, Department of Engineering; *R. Karri,* Center for Cyber Security, Department of Electrical and Computer Engineering; *K. Chakrabarty,* Arizona State University

SESSION C3
Challenges to Enable an Immersive and Inclusive Metaverse (Special Session)
Magic Kingdom Ballroom 3
C. Metra, Università di Bologna (Chair)

C3.1 Addressing Metaverse Hardware Reliability challenges with Silicon Lifecycle Management
J. Athavale, Y. Zorian, Synopsys

C3.2 Bridging Technology and Humanity to Cultivate an Inclusive Metaverse
J. Ranaweera, IEEE

C3.3 Successes and Challenges of Making the Metaverse Accessible Everywhere and for Everyone
N. Leung, B. Vrcelj, I. Bouazizi, P. Tinnakornsrisuphap, P. Hande, T. Stockhammer, Qualcomm

SESSION D3
TTTC PhD Competition
Magic Kingdom Ballroom 4
M. Portolan,Grenoble-INP (Chair)

D3.1 Understanding and Improving GPUs' Reliability Combining Beam Experiments with Fault Simulation
** F. Santos,* UFRGS/Univ Rennes INRIA; *L. Carro,* Instituto de Informatica / UFRGS; *P. Rech,* UFRGS/University of Trento

D3.2 A Full-Stack Approach for Side-Channel Secure ML Hardware
** A. Dubey, A. Aysu,* North Carolina State University

D3.3 Towards Robust Deep Neural Networks against Design-time and Run-time Failures
** Y. Li, Q. Xu,* The Chinese University of Hong Kong

2:00 p.m. – 2:40 p.m.

SESSION V1
Visionary Talk
Disney Grand Ballroom Center
T. McLaurin, ARM (Chair)

V1.1 Four Wheels and A Billion Lines of Code - Enabling the Future of Automotive
D. Vachani, ARM

2:40 p.m. – 4:00 p.m.

SESSION DEI
DEI Panel
Disney Grand Ballroom Center
A. Anderson, AMD (Moderator)

4:30 p.m. – 6:00 p.m.

SESSION A4
AI 2
Magic Kingdom Ballroom 1
K. Chakrabarty, Arizona State University (Chair)

A4.1 High-Speed, Low-Storage Power and Thermal Predictions for ATPG Test Patterns
*Z-J. Liang, Y-T. Wu, * Y-F. Yang, J-M. Li,* Graduate Institute of Electronics Engineering National Taiwan University; *N. Chang, A. Kumar, Y-S. Li,* Ansys Inc.

A4.2 Scan Cell Segmentation based on Reinforcement Learning for Power-Safe Testing of Monolithic 3D ICs
** S-C. Hung, A. Chaudhuri,* Duke University; *S. Banerjee,* NVIDIA Corporation; *K. Chakrabarty,* Arizona State University

A4.3 Improving Productivity and Efficiency of SSD Manufacturing Self-Test Process by Learning-based Proactive Defect Prediction
** Y. Gu, X. Wang, Z. Chen, C. Wu, X. Guo, J. Li, M. Guo,* Shanghai Jiao Tong University;*S. Wu, R. Yuan, T. Zhang,* Beijing Memblaze Technology Co., Ltd.; *Y. Zhang, H. Cai,* Huawei Technologies Co., Ltd.

SESSION B4
Emerging 2
Magic Kingdom Ballroom 2
S. Adham, TSMC (Chair)

B4.1 Magnetic Coupling Based Test Development for Contact and Interconnect Defects in STT-MRAMs
** S. Yuan, Z. Zhang, M. Fieback, H. Xun, M. Taouil, S. Hamdioui,* Delft University of Technology; *E. Marinissen, G. Kar, S. Rao, S. Couet,* IMEC

B4.2 Device-Aware Test for Ion Depletion Defects in RRAMs
** H. Xun, S. Yuan, M. Fieback, M. Taouil, S. Hamdioui,* Delft University of Technology; *H. Aziza,* Aix Marseille University

B4.3 Analysis and Characterization of Defects in FeFETs
** D. Thapar, A. Chaudhuri,* Duke University; *S. Thomann, H. Amrouch,* University of Stuttgart; *K. Chakrabarty,* Arizona State University

SESSION C4
AI Functional Safety
Magic Kingdom Ballroom 3
M. Tahoori, Karlsruhe Institute of Technology (Commentary)

C4.1 Functional Safety of Spiking Neural Network VLSI Implementations
***** *H-G. Stratigopoulos,* Sorbonne, CNRS

C4.2 Safety of AI and AI for Safety: From CMOS to Emerging Technologies in Neural Networks
***** *S. Di Carlo,* Politecnico di Torino

C4.3 Managing Safety & Reliability of AI Chips throughout the Lifecycle
**Y. Zorian,* Synopsys

SESSION D4
Panel: AI in EDA and Test
Magic Kingdom Ballroom 4
J. Rearick, AMD (Commentary)
AI for the Front-end (DFT, ATPG, Fault Simulation)
K. Chakravadhanula, Cadence Design Systems
R. Singhal, Synopsys
R. Press, Siemens
AI for the Back-end (Diagnosis, Debug, Yield Enhancement)
N. Hanchate, Cadence Design Systems
G. Cortez, Synopsys
J. D'Souza, Siemens
.

10:30 a.m. – 12:00 p.m. Pacific Daylight Time

*: Paper presenter

SESSION A5
Automotive
Magic Kingdom Ballroom 1
Chen He, NXP (Chair)

A5.1 Enhanced ML-based Approach for Functional Safety Improvement in Automotive AMS Circuits
*A. Arunachalam, * S. Das, M. Rajan, K. Basu,* University of Texas at Dallas; *F. Su, A. Raha, S. Natarajan,* Intel Corporation; *X. Jin,* NXP Semiconductors; *S. Banerjee,* NVIDIA Corporation

A5.2 Preventing Single-Event Double-Node Upsets by Engineering Change Order in Latch Designs
*M-H. Hsiao, H-Y. Tsai, * L. P-T. Wang, C-W. Liang, C-P. Wen, H. Chiueh,* National Yang Ming Chiao Tung University

A5.3 Measuring Non-Redundant VIA Test-Coverage for Automotive Designs in Lower Process Nodes
** S. Ramesh, R. Kalyan, J. Yanez,* NXP Semiconductors; *A. Glowatz, M. Ryynaenen, S. Schwarz,* Siemens

SESSION B5
Post Silicon 1
Magic Kingdom Ballroom 2
J. Rajski, Siemens (Chair)

B5.1 Diagnosis of Systematic Delay Failures through Subset Relationship Analysis
*B-H. Hsieh, * Y-S. Liu,* National Taiwan University; *J-M. Li,* Graduate Institute of Electronics Engineering National Taiwan University, Taipei; *C. Nigh,* Qualcomm Technologies, Inc.; *M. Chern,* Qualcomm Semiconductor Limited, Hsinchu;*G. Bhargava,* Qualcomm India Private Limited

B5.2 Predicting the Resolution of Scan Diagnosis
M. Devendhiran, Intel Corporation; ** J. Janicki, S. Urban, M. Sharma, J. D'Souza,* Siemens DISW

B5.3 Predictor BIST: An "All-in-One" Optical Test Solution for CMOS Image Sensors
** J. Lefevre, P. Debaud,* STMicroelectronics; *P. Girard, A. Virazel,* LIRMM

SESSION C5
CHIPS Act Panel
Magic Kingdom Ballroom 3
J. Rearick, AMD (Commentary)

SESSION D5
Silent Data Corruption: Leveraging RAS for the Fleet Health
Magic Kingdom Ballroom 4
Y. Zorian, Synopsys (Commentary)

D5.1 Fleet Health and Silent Data Corruptions in Meta Infrastructure
H. Dixit, Meta

D5.2 Could Standardizing RAS Requirements Impact Silent Data Corruption?
Y. Zorian, J. Athavale, Synopsys

D5.3 Harnessing the Power of Microarchitectural Modeling for Fast Prediction of SDC rates throughout Silicon Lifetime
D. Gizopoulos, University of Athens

1:30 p.m. – 3:00 p.m.

SESSION A6
Security
Magic Kingdom Ballroom 1
S. Blanton, Carnegie Mellon University (Chair)

A6.1 ARC-FSM-G: Automatic Security Rule Checking for Finite State Machine at the Netlist Abstraction
** R. Kibria, F. Farahmandi, M. Tehranipoor,* University of Florida

A6.2 Laser Fault Injection Vulnerability Assessment and Mitigation with Case Study on PG-TVD Logic Cells
*R. Holzhausen, * T. Farheen, M. Thomas, N. Maghari, D. Forte,* University of Florida

A6.3 Simply-Track-And-Refresh: Efficient and Scalable Rowhammer Mitigation
** E. Ortega, T. Bletsch, J. Talukdar, W. Paik,* Duke University; *B. Joardar,* University of Houston; *K. Chakrabarty,* Arizona State University

SESSION B6
Post Silicon 2
Magic Kingdom Ballroom 2
P. Song, IBM (Chair)

B6.1 Low-cost Production Scan Test for Compression-based Designs
*B. Nandakumar, S. Chillarige, * B. Archer,* Cadence Design Systems

B6.2 Enhancing Good-Die-in-Bad-Neighborhood Methodology with Wafer-Level Defect Pattern Information
** C-M. Liu, C-H. Yen, S-W. Lee, K-C. Wu, M. Chao,* National Chiao Tung University

B6.3 Enabling In-field Parametric Testing for RISC-V Cores
*S. Ghasemi, S. Meschkov, J. Krautter, D. Gnad, *M. Tahoori,* Karlsruhe Institute of Technology

SESSION C6
Panel: Will Silent Data Errors give a new lease on Life to Semiconductor Test?
Magic Kingdom Ballroom 3
V. Chickermane, Siemens (Commentary)

SESSION D6
ITC India
Magic Kingdom Ballroom 4
C. H-P Wen National Yang Ming Chiao Tung University (Chair)

D6.1 Power Domain Aware DFT Implementation
S. Singhal, *S. Mukherjee, C. Papameletis, K. Chakravadhanula, Ankit Bandejia, Dale Meehl, Archana Vyas, Mohan Gandla,* Cadence

D6.2 Analysis of Non-idealities in On-chip Loopback Testing of Data Converters
T. Mandal, Indian Institute of Science; *A. R, R. Parekhji,* Texas Instruments

D6.3 Bridging Repairability Gaps in Shared Bus Architecture with Shared Physical Memory Implementation
N. Karkare,,W. Pradeep, Google

Wednesday, 12:30 p.m. – 2:30 p.m. Pacific Daylight Time

PO.1 An Optimized Thermal Control Methodology for Burn-In and Qualification Stress on Automotive MCUs/MPUs
C. He, V. Vu, D. Grover

PO.2 BIST for Arm's 3nm Multi-Port Register Files
A. Chen, V. Choserot, M. Kumar, K. Gelda, S. Dixit, B. Nadeau-Dostie, W. Zou, J. Yun, H. Kodali, A. Au, L. Schramm

PO.4 Automatic Generation and Validation of System Verilog Assertions from Natural Language Specifications
F. Aditi, M. Hsiao

PO.5 Deploying Cutting-edge Adaptive Test Analytics Apps Based on a Closed-loop Real-time Edge Analytics and Control Process Flow into the Test Cell
G. Cortez, K. Butler,

PO.6 Transfer Learning in MCU Performance Screening
N. Bellarmino, R. Cantoro, U. Schlichtmann, G. Squillero, T. Kilian, M. Huch

PO.7 Machine Learning Enhanced Kernel Based Cluster Fault Analysis
C. He, R. Chen

PO.8 Optimization of Scan VMIN Capability Grouping for Enhanced Defect Detection
T. Jacobs, N. Nguyen, M. Crain, M. Han

PO.15 On-Chip Delay Measurement for Degradation Detection and Prediction
Y. Miyake, T. Kato, S. Matsunaga, H. Futami, M. Aso

PO.16 Leveraging Deep Learning to Predict Memory Faults from Hardware Architectures
P. Daniel,

PO.17 Validation of Ultra-low Jitter-Reduction Techniques up to 20 GHz
D. Keezer, D. Minier, H. Li

PO.18 Power, Timing and Physically Aware Test points Exploration at RTL
N. De Sainte Marie, C.Aktouf, V. Boyer, O. Florent, M. Kogan

PO.19 Scan Diagnosis On The Cloud
J. Abraham, S. Springall, S. Shindgi, J. D'Souza, R. Klingenberg

PO.20 ATE Integration of High Performance, High Data Rate 3rd Party Instruments for Reliable Manufacturing Test
T. Lyons

PO.21 Scan Channel Configuration Selection using ML for Test Metric Prediction
P. K. Rukmangada, M. Farkash, R. Malhotra, E. C. Chan, A. Margulis, T. Payakapan

PO.22 Inverse mapping Scan Diagnosis with Transformer Neural Networks
P. Daniel

PO.23 Structural Tests over HSIO on SLT (ATS 7038)
A. Patel, S. Ganta, R. Allen

PO.24 Teradyne's PortBridge Expedites Complicated SOC Debug by Integrating Comprehensive Industry Tools
R. Fanning, S. Molavi, C. Clark, S. Peck

PO.25 General Purpose ATE Software
R. Dokken, G. Chan

PO.26 Memory test automation using shared bus interface aids with turnaround time
P. Seetharaman, A. Au, S. Bromberek

PO.27 Automotive ASIC Test time reduction with Observation Scan Technology (OST)
A. S Harith, J. Mayer, N. Mukherjee, V. Nath S, V. Pavan, M. Rawal

PO.28 Effective Yield Boost and Cost Saving by Volume Diagnosis using Yield Explorer
T. C.Y. Liu, T-W. Shao, A. P.H. Tseng, J. Z.J. Lin, J. Y.J. Chiu, E. H.Y. Chou, K-Y Hsu

PO.29 Cell-Aware Failure Analysis: Advanced Cell-Aware Techniques to Identify the FEOL/MOL Layer Systematic Defects in Cutting-edge Technology
J. Park, H. Lim, Y. Son, D. Han, J. Park, Y. Lee, C. Hora, R. Guo

PO.30 Test Scalability with Sequential Compression Technology
M. Nathan, L. Chen, T. Ngo, M. Chau, L. K. Ramachandra,,Bala Tarun Nelapatla

PO.31 Test Robustness and Glitch Detection with TestMAX Advisor
R. Koneru, R. Allen, A. Jindal, D. Varadhan

PO.32 Advanced Test Point and Wrapping Techniques for Automotive Designs
R. Koneru, R. Allen, G. Shofner, C. Falk

PO.33 Physical Connection Aware SMS BIST Implementation for Abutted Design
M. Nath, M. M. Junjawadkar, D. Kim, M. Arora

PO.34 Holistic Approach to Solving Silent Data Corruption
A. Cron, R. Allen

PO.35 Deep Silicon Data and Analytics for Lifelong Safety and Reliability
D. Alexandrescu, L. Kennedy, R. Allen, J. Davoudi, P. Mahajan

PO.36 The Importance of Sensor Analytics in Enabling Silicon Lifecycle Management
M. Laird, R. Allen

PO.37 Dynamic Power Reduction for Hierarchical Test
S. Singhal, S. Ravichandran, K. Chakravadhanula, S. Mukherjee

PO.38 Extended Feature Testing using MBIST
P. Arora, N. Sharma, C. Wisnesky

PO.39 Pre-Silicon Estimation of Scan Chain Diagnosability
J. Singh, B. Nandakumar, S. Chillarige, V. Mishra

PO.40 Efficiency of Packetized Data Delivery in 2.5D/3D Designs
P. Orlando, K. Grubich, M. Czartorysk

PO.41 Adaptive DFT technology in use with Automated Test Equipment (ATE)
P. Orlando, K. Grubich

PO.42 RTL DFT Analysis and Insertion of Test Points at RTL
J. Mayer, N. Mukherjee, O. Laouamri

PO.43 Clocking (DFT) Considerations in Designs with Packetized Scan Data
J. Kaur, R. Press, Siemens

Monday 4:30 p.m. – 6:00 p.m. PDT

Panel 1 – Grand Challenges in Test

Moderator: Anne Gattiker

The ITC'23 Program Committee is taking some inspiration from the Physics community for our opening panel on Monday afternoon: every decade, the US National Research Council publishes a short list of the "grand challenges" in the discipline which then drives planning, research, and funding. This approach has spread to other organizations, including the National Academy of Engineering, which has a list of 14 such challenges.

We'll get in on the action with an interactive town hall session that aims to articulate the "grand challenges of test" that our community can use to help guide the direction of innovation in our world. Dr. Anne Gattiker from IBM Research will facilitate the discussion with some prompting from a few experts to elicit input from the entire audience. Here's your chance to make your voice heard and be part of an incredibly exciting time in our industry.

Panelists:

- S. Blanton
- P. Nigh
- J. Carulli
- I. Pomeranz
- J. Rearick

Wednesday 2:40 p.m. – 3:30 p.m. PDT

Panel 2: Allyship in the test community: a real-world guide to DEI Vision

Organizer: *J Rearick,* AMD
Moderator: *A. Anderson*
Panelists:

- *S. Blanton,* Carnegie Melon
- *T. McLaurin,* ARM
- *C. Roos,* Roos Instruments

The test community is a diverse one, yet many of us may not be familiar with either the subtleties or the complexities of how best to work in such an environment. In this moderated panel session, we'll hear several of our test colleagues tell their stories and give us practical suggestions on how we can be better allies, help members of under-represented groups get a better foothold, and create more welcoming and inclusive workplaces. In contrast to (often counterproductive) DEI compliance training, this session focuses on the narratives from people you know in our community and steps you can take to become a more aware coworker.

Wednesday 4:30 p.m. – 6:00 p.m. PDT

Panel 3: Session D4: AI in EDA and Test

The explosion of Artificial Intelligence applications has already touched the design and test communities and may be poised to fundamentally change the way that we test engineers approach our jobs. The panelists in this session will catalog some of the existing tasks where AI has made an impact, then speculate on others that may be next on the list. The underlying question that the discussion with the audience will seek to answer is "Will AI take my job away -or- make me better at doing my job?"

Moderator: *J. Rearick,* AMD
Panelists:

- *N. Hanchate*, Cadence Design Systems
- *R. Singhal,* Synopsys
- *G. Cortez,* Synopsys

Thursday 10:30 a.m. – 12:00 p.m. PDT

Panel 4: Session C5: The CHIPS Act

Organizer: *J Rearick,* AMD
Moderator: *J. Rearick,* AMD
Panelists:

- *A. De La Serna*, Siemens
- *J. Hoganson,* AMD
- *J. Caruli,* Global Foundries
- *S. Iyer*, Director of the CHIPS R&D National Advanced Packaging Manufacturing Program

$52 billion from the US CHIPS Act and €43 billion ($47 B) from the EU Chips Act is a lot of money flowing into the semiconductor business. How will it be spent? Besides the foundries, will there be a portion available to the design and test sectors? What is the status of these programs and how can we learn more about them? The experts on our panel will share their knowledge and experience.

Thursday 1:30 p.m. – 3:00 p.m. PDT

Panel 5: Session C6: Will Silent Data Errors give a new lease on life to Semiconductor Test?

Organizers: *Vivek Chickermane, Nilanjan Mukherjee***,** Siemens DISW
Moderator: *Anne Meixner***,** Semiconductor Engineering
Panelists:

- Sandeep Bhatia (Google)
- Sankar Gurumurthy (AMD)
- David P. Lerner (Intel)
- Jennifer Dworak (SMU)
- Janusz Rajski (Siemens DISW)
- Noam Brousard (protean Tecs)

Silent Data Errors (aka Silent Data Corruption) has garnered significant attention in the last couple of years emerging from relative obscurity over the previous two decades. At ITC 2022, there was near unanimous agreement in the Test community that the topic of Silent Data Errors (SDE) is one of the biggest test challenges now and in the foreseeable future. Most of the focus of the Test Community in the past has been on achieving extremely high-test quality at time t=0, relying on extensive DFT methodologies and design rule checks to achieve high test coverage coupled with advanced ATPG techniques to minimize test escapes and field returns. With wide-spread deployment of leading-edge semiconductor products in high-dependability and mission critical applications that also have a long field life any latent defects, test escapes, design marginalities, and aging related degradation may result in SDEs..

IEEE Computer Society Test Technology Technical Council Workshops

Thursday and Friday

General Workshop Information

Two workshops are being held in parallel immediately following ITC 2023. They will each start with an opening address on Thursday afternoon, October 12, followed by a technical session. The remaining technical sessions will be held on Friday, October 13. The technical scope of each workshop is described below.

Workshop Registration

All workshop participation requires registration. To register in advance for one of the workshops, do so online. Discount workshop registration rates apply until September 1, 2023. Workshop registration includes the opening address, technical sessions, and a digest of papers.

Workshop Schedule

The two workshops will adhere to the same schedule:

Thursday, October 12		Friday, October 13	
Plenary1, Keynote:	4:00 p.m. – 5:00 p.m.	Technical Sessions	8:00 a.m. – 4:00 p.m.
Technical Sessions:	5:00 p.m. – 6:30 p.m.		

Workshop Reception: Thursday October 12, 7:00 p.m. – 9:00 p.m.

Note: Workshop schedule is subject to change

Digest of Papers

A digest of papers will be distributed only to attendees at the workshops as an informal proceedings.

Further Information

For more information on the workshops contact their organizers by e-mail or check the TTTC Web site http://ieee-tttc.org

ARTS 2023: IEEE Automotive Reliability and Test & Safety Workshop 2023

Automotive electronics is becoming more and more relevant in daily life, especially with the advent of autonomous driving. People will become 100% dependent on the proper operation of electronic systems. The ARTS Workshop will focus on test, reliability, and safety of automotive electronics, including IC design, test development, system-level integration, production testing, in-field test, diagnosis and repair solutions, cybersecurity, as well as architectures and methods for reliable, safe, and secure operation in the field.
The ARTS Workshop wants to offer a forum for industry specialists and academic researchers to present and discuss these challenges and emerging solutions. This eighth edition will take place in the frame of the IEEE International Test Conference (ITC) and is sponsored by the Test Technology Technical Council (TTTC) of the IEEE Computer Society.

See the ART2023 Web Page for more information on ARTS..

General Chair: Yervant Zorian zorian@synopsys.com
Program Chair: Paolo Bernardi paolo.bernardi@polito.it
ART Web Page: https://cas.polito.it/ARTS2023/

Location: Magic Kingdom Ballroom 1

Third IEEE International Workshop on Silicon Lifecycle Management (SLM)

With increasing system complexity, security, stringent runtime requirements for functional safety, and cost constraints of a mass market, the reliable and secure operation of electronics in safety-critical, enterprise servers and cloud computing domains is still a major challenge.

While traditionally design time and test time solutions were supposed to guarantee the in-field dependability and security of electronic systems, due to complex interaction of runtime effects from running workload and environment, there is a great need for a holistic approach for silicon lifecycle management, spanning from design time to in-field monitoring and adaptation.

Therefore, the solutions for lifecycle management should include various sensors and monitors embedded in different levels of the design stack, access mechanisms and standards for such on-chip and in- system sensor network, as well as data analytics on the edge and in the cloud.

The SLM Workshop offers a forum to present and discuss these challenges and emerging solutions among researchers and practitioners alike.
SLM will take place in conjunction with the IEEE International Test Conference (ITC2023,) is sponsored by IEEE Philadelphia Section and is conceived by the IEEE Test Technology Technical Council (TTTC).

General Chair: Yervant Zorian zorian@synopsys.com
Program Chair: Mehdi Tahoori

SLM Web Page: https://people.rennes.inria.fr/Marcello.Traiola/SLM23/

Location: Magic Kingdom Ballroom 4

IEEE TPTR - Top Picks in Test and Reliability

“Top Picks in VLSI Test and Reliability” is a workshop that collects and presents the most impactful publications in the past 6 years in the areas of VLSI test and reliability.

Co-Chairs:
Jyotika Athavale, President-Elect, IEEE Computer Society (US)
Haralampos-G. Stratigopoulos, Sorbonne Université, CNRS, LIP6 (FR)

TPTR Web Page: https://people.rennes.inria.fr/Marcello.Traiola/TPTR2023/
Location: Magic Kingdom Ballroom 3

ITC 2023 is taking place the week of October 8-13, 2023. Attend in person to get the most out of the event and interact with presenters, exhibitors, and more. However, for those who cannot attend in person, we offer a virtual option, both for the main conference and for tutorials.

Guide to accessing and using the virtual platform

- An email with a password-creating link was distributed by Underline to all registered ITC 2023 attendees to make it easy for first-time users of Underline to create the password for their respective accounts (**named by email address used when you registered**!). If you have an Underline account already, from a previous ITC year, you will be prompted to login to your existing account.
- When the Underline site for ITC2023 is turned on, all at-conference and virtual registrants will be sent an email giving the link to the site, with instructions on how to access it. Underline provides a mobile-friendly conference schedule, which you can use even if you are on-site and are viewing presentations live. This will also give you access to recordings of presentations, which you can review after the conference is over.
- Tutorial-only and workshop-only registrants will get access to tutorials and workshops only, and will not be able to access the ITC conference, including panels, papers, and plenaries.

Registration Categories

Register Online

All Test Week activities require a registration badge for admittance. There are three registration periods with differing fees

- Early discount preregistration through September 1, 2023
- Non-discount preregistration September 2 to October 6, 2022 .

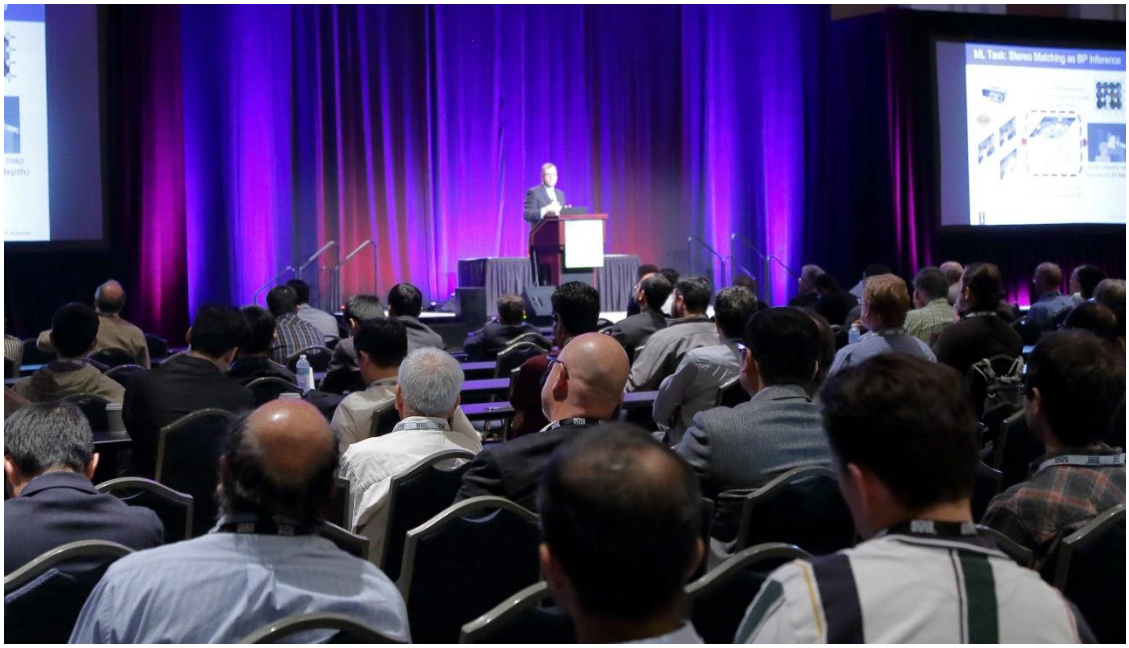
▶ITC Full-Conference Registration Includes ITC technical paper and panel sessions, exhibits, and access to ITC 2023 papers, slides and presentations for one month after the conference. Registration does not include the tutorials on Sunday and Monday or the workshops on Thursday and Friday.

▶Tutorial Registration Tutorials are a half-day in length.
One-Day tutorial registration fee is for two tutorials—a morning tutorial and afternoon tutorial, both on the same day, e.g., Tutorial 1 and Tutorial 4 on Sunday. You may register for up to four tutorials (two consecutive on Sunday and two consecutive on Monday).
All-Access Pass tutorial registration provides in-and-out access to all twelve tutorials over both days.

All registrations include study material, breaks and lunches on the day(s) attended. Tutorial registration does not include the ITC technical program, ITC receptions, exhibits, exhibit hall lunches, ITC publications, ITC giveaways or the workshops on Thursday and Friday.

▶Workshop Registration Includes the items specified on page 23. Registration does not include the ITC technical program, exhibits, or the tutorials on Sunday and Monday.

▶Discount Rates Early registration rates apply only when you complete your registration by September 1, 2023, either online or with a paper form and payment postmarked or faxed by September 1, 2023. To receive IEEE member or student member reduced rates, you must include your member number, which will be verified.



Registration Fees

Early Preregistration Rates (on or before September 1, 2023)

Early Discount Preregistration Fees	Full ITC Conf	One Day 2 Tutorials	All-Access Tutorial Pass	One Workshop
IEEE/CS Member	$875	$275	$540	$275
Nonmember	$1095	$345	$675	$345
IEEE/CS Member, student or Life	$325	$250	$490	$250
Nonmember, student	$410	$315	$615	$315

Late Preregistration Rates (after September 1, 2023)

Late Preregistration Fees	Full ITC Conference	One Day 2 Tutorials	All-Access Tutorial Pass	One Workshop
IEEE/CS Member	$1155	$325	$590	$300
Nonmember	$1445	$410	$740	$375
IEEE/CS Member, student or Life	$325	$290	$530	$275
Nonmember, student	$410	$365	$665	$345

There are additional registration options for Program Participants and Virtual attendees. See http://www.itctestweek.org/register/ for full details.

Refunds

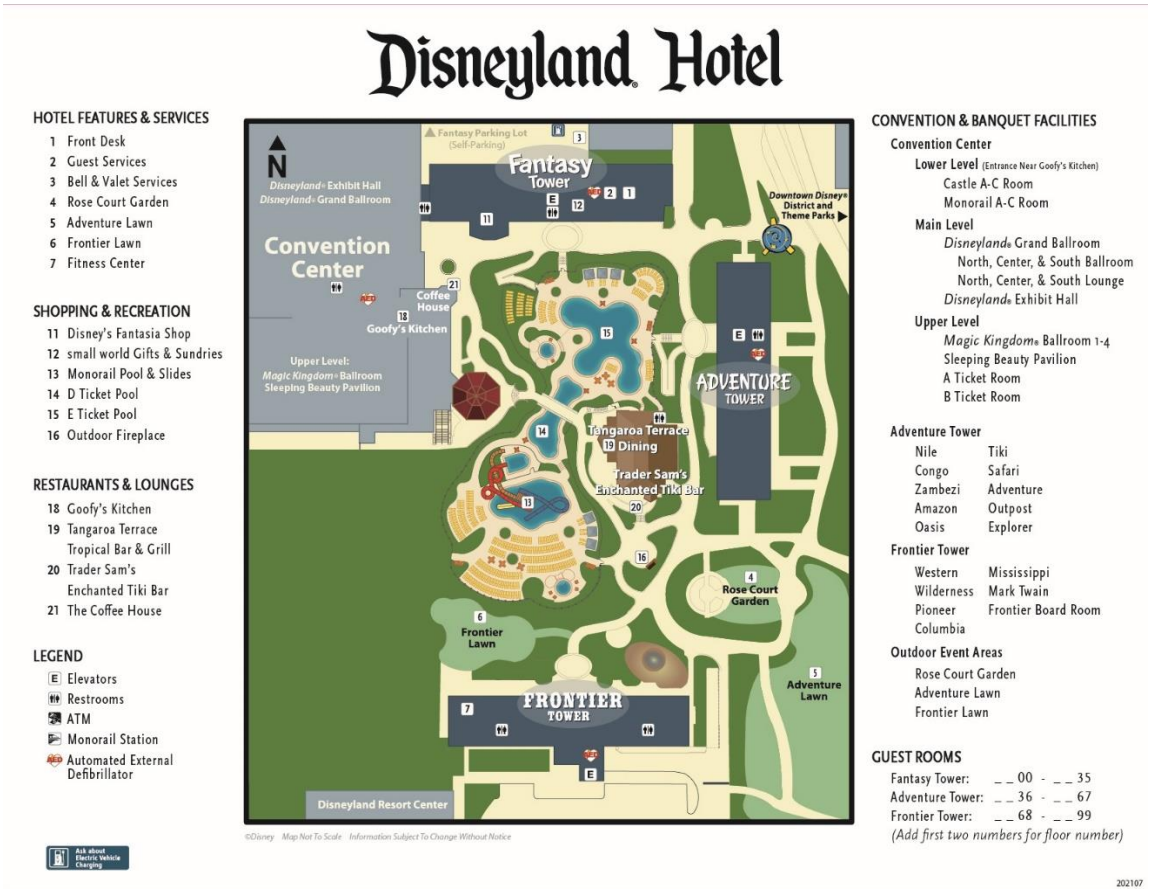
All refund/cancellation requests must be received in writing to registration+ITC@computer.org by **29 September 2023, 11:59 PM Eastern Time.** There will be an administrative fee of **US$10** for cancelled registrations

Venue

ITC 2023 is taking place at the Disneyland Hotel, Anaheim, California.

The Hotel address is:

1150 West Magic Way
Anaheim, California 92802



1. The ITC Final Program release 1.0 was generated with Adobe Acrobat 8.2.6 on October 2, 2023

2. The program will be updated periodically as new material is available - check back often.

3. Navigate using the tabs and links at the top of each page.

4. Use underlined links in the At-a-Glance to find specific items.

5. For more information contact:

Subject	Contact	Email
Advance Program	**Scott Davidson**	*davidson.scott687@gmail.com*
Corporate Forum	**Chen-huang Chiang**	*chen-huan.chiang@intel.com*
Exhibits and Exhibiting	**Chen-huang Chiang**	*chen-huan.chiang@intel.com*
Fringe Technical Meetings	**IEEE Computer Society**	*ieeeitc@computer.org*
Posters	**Jeff Rearick**	*Jeff.Rearick@amd.com*
Registration	**IEEE Computer Society**	*ieeeitc@computer.org*
Technical Program	**Jeff Rearick**	*Jeff.Rearick@amd.com*
TTTC Tutorials	**Yervant Zorian**	*zorian@synopsys.com*
TTTC Workshops	**Yervant Zorian**	*zorian@synopsys.com*
All Other Questions	**IEEE Computer Society**	*ieeeitc@computer.org*

Attendance at, or participation in, this conference constitutes consent to the use and distribution by IEEE of the attendee's image or voice for informational, publicity, promotional and/or reporting purposes in print or electronic communications media.
.

Photographs of copyrighted PowerPoint or other slides are for personal use only and are not to be reproduced or distributed. Do not photograph any such images that are labeled as confidential and/or proprietary.