INTERNATIONAL TEST CONFERENCE

AI Toward Autonomous Testing

OCTOBER 28 - NOVEMBER 2, 2018
Co-located with ISTFA 2018
PHOENIX CONVENTION CENTER
PHOENIX, ARIZONA

Call for Papers

International Test Conference is the world's premier venue dedicated to the electronic test of devices, boards and systems—covering the complete cycle from design verification, design-for-test, design-for-manufacturing, silicon debug, manufacturing test, system test, diagnosis, reliability and failure analysis, and back to process and design improvement.

ITC 2018 is co-located with International Symposium for Testing and Failure Analysis (ISTFA). The theme of ITC 2018 is Artificial Intelligence (AI) Toward Autonomous Testing, where the term AI includes a broad range of optimization, machine learning, and domain-specific techniques for enhancing the extent of test automation toward the ultimate goal of "Autonomous Testing." ITC 2018 also includes three application-specific tracks, Automotive, Security and Failure Analysis/Yield Learning, where multiple sessions will be allocated for each track.

Authors are invited to submit original, unpublished papers describing recent work in the field of test and design. Of particular interest are works dedicated to the topics listed on the right and/or works related to the conference theme and/or works focused on the special tracks. Authors are also invited to submit practical, industry best practices. Submissions simultaneously under review or accepted by another conference, symposium or journal, will be summarily rejected.

Submissions must include:

- Title of paper.
- Name, affiliation, e-mail address of each author.
- The corresponding author(s). ITC will communicate with the corresponding author(s).
- One or two topic(s) from the topic list, or a description of your topic.
- An electronic copy of a complete paper up to **10 pages,** or an extended summary up to **six pages**. **Submissions less than four pages are rarely accepted.**
- An abstract of 35 words or less to be entered online.

ITC maintains a competitive selection process for technical papers. Submissions must clearly describe the status of the reported work, its contribution, novelty and/or significance. Supporting data, results (priority is often given to papers with results from real designs) and conclusions, and references to prior work must also be included. ITC does not accept submissions that do not meet the specified criteria. Submit at - https://easychair.org/conferences/?conf=itc2018.

Paper title/abstract due:	**March 23, 2018**
Paper final PDF due:	**April 6, 2018**
Author notification:	**June 1, 2018**
Final manuscript due:	**August 3, 2018**

Authors are also invited to submit a **single-page** poster proposal. Posters are a useful way of presenting late-breaking results, getting feedback on an innovative method, or participating without having to write a full paper. Acceptance as a poster does not preclude submission of a more complete work as an ITC paper in 2019. Additional information on poster abstracts and submissions can be found under the author link on the program web site.

Poster submission deadline:	**June 15, 2018**
Author notification:	**July 13, 2018**

Test Week tutorial and workshop proposals are also welcomed. Deadlines and other information about proposals can be obtained from TTTC at: http://tab.computer.org/tttc

For detailed information about the submission process, requirements and deadlines, the selection process and any other questions regarding the program itself or contact information, please consult the ITC web site at http://www.itctestweek.org

For information about ISTFA see http://www.istfa.org

ITC invites submissions on the latest advances in test, validation and diagnosis of ICs, boards and systems.

Topics of interest include
(but not limited to)**:**

3D/2.5D Test
Adaptive Test in Practice
ATE/Probe Card Design
Advances in Boundary Scan
Bring-Up
Data Driven Methods
Data Exchange and Infrastructure
Defect-oriented Testing
DFM and Test
Diagnosis
Economics of Test
End-to-End Data Analysis
End-to-End System Security
Embedded BIST and DFT
Emerging Defect Mechanisms
Hardware Security and Trust
IoT Testing
Jitter, High-Speed I/O and RF Test
Known-Good-Die testing
Memory Test and Repair
MEMS Testing
Mixed-Signal and Analog Test
New Technologies and Test
On-Chip Test Compression
Online Test
Pre-Silicon Verification
Post- Silicon Validation
Power Issues in Test
Protocol-aware Test
Reliability and Resilience
Scan Based Test
SoC/SiP/NoC Test
Silicon Debug
Simulation and Emulation
System Test (Applications)
System Test (Hardware/Software)
Test-to-Design Feedback
Test Escape Analysis
Test Flow Optimizations
Test Generation and Validation
Test Resource Partitioning
Test Standards
Test Time Analysis and Reduction
Testing High Speed Optics/Photonics
Timing Test
Yield Analysis and Optimization

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