2022

INTERNATIONAL TEST CONFERENCE

september 25-30, 2022

hybrid | disneyland/anaheim, ca

WELCOME

ITC is the world's premier conference dedicated to electronics test. This year's ITC continues with its mission to play a unique role as an **information sharing forum,** where the wide range of its offerings allows ITC participants to learn, network and conduct business. This year's program includes a top-notch technical program, vibrant exhibitors, information-packed **tutorials**, interactive technical **panels**, two focused **workshops**, as well as the all-important networking that these events can provide. The technical program has been designed to optimize personal interactions on all levels. This year's program will include papers from a pool of impressive submissions and solicited papers. Of these submissions, a large number will focus on AI, automotive, memory, and hardware security. In complement to the paper presentations, there will be special sessions on hardware security certification, chiplet integration, silicon lifecycle management, computing in memory, as well as design and test of high-power compound devices and quantum electronics.

We are continuing and expanding on the inclusion of the Industrial Practice papers sessions as ITC has a very strong focus on industry practice as well as industry and academia advances. The three **keynotes** will encompass the past, present and future of our industry. In addition, there will be a **visionary talk** on AI accelerators.

ITC 2022 features a vibrant **exhibition** showcasing relevant companies. The exhibition will serve as a convenient one-stop-shop for all the elements of test technology.

In the past 53 years, ITC has helped globalize our industry and wants to continue to do so in the future. This year's return to a live event will enable us to embrace all the features of the conference we have missed such as personal interaction.

ADMISSION TO ITC AND TEST WEEK ACTIVITIES

A personal registration badge is required for admission to all Test Week™ Activities.

LOCATION OF EVENTS

ITC Test Week 2022 events will take place at the Disneyland Hotel, Anaheim, CA. Check the Technical Session listings for session locations.

PANEL SESSIONS

ITC encourages the free exchange of ideas in panel sessions. Opinions in these sessions are often in a formative stage and do not represent completed work or the official position of the speaker or of his or her company. Panel sessions are "off the record"—what is said in them is not for quotation or attribution. Tape recorders and cameras are not permitted.

PHOTOGRAPHY AND RECORDINGS

Attendance at, or participation in, this conference constitutes consent to the use and distribution by IEEE of the attendee's image or voice for informational, publicity, promotional and/or reporting purposes in print or electronic communications media.

Video recording by participants and other attendees during any portion of the conference is not allowed without special prior written permission of IEEE.

Photographs of copyrighted PowerPoint or other slides are for personal use only and are not to be reproduced or distributed. Do not photograph any such images that are labeled as confidential and/or proprietary.

REGISTRATION FOR ALL EVENTS

ITC registration counter at the Disneyland Hotel

Sunday: 7:30 am – 3:00 p.m.	Monday: 7:30 a.m. – 5:00 p.m.
Tuesday: 8:00 a.m. – 6:00 p.m.	Wednesday: 8:00 a.m. – 4:00 p.m.
Thursday: 8:00 a.m. – 3:00 p.m.	Friday: 7:30 a.m. – 12:00 p.m.

Registration is closed 12:00 – 1:00 p.m. Tuesday – Thursday, 11:00 a.m. – 1:00 p.m. Sunday, Monday

HIGHLIGHTS

TTTC TUTORIALS
TTTC presents 12 half-day tutorials on Sunday and Monday.

MONDAY PANEL
An Industry-wide Dialog on Chiplets and Heterogeneous Integration

KEYNOTE TALKS
Keynotes on Tuesday, Wednesday and Thursday.

VISIONARY TALKS
One Visionary Talk Wednesday.

TECHNICAL SESSIONS
22 technical paper sessions Tuesday – Thursday

SPECIAL SESSIONS
10 special sessions Tuesday – Thursday

ITC WELCOME RECEPTION
All ITC registered full-conference attendees and exhibitors are invited to attend on Tuesday from 6:00 p.m. to 8:00 p.m.

POSTER SESSIONS
View 36 posters in the exhibit hall.

CORPORATE FORUM
The latest technical innovations from our exhibitors and corporate supporters.

WORLD-CLASS EXHIBITS
See the latest technology on the exhibit floor.

EXHIBITS PASSPORT PROGRAM
Visit company booths to be eligible for prizes.

COMPLIMENTARY EXHIBIT HALL LUNCHES
Tuesday, Wednesday and Thursday for full-conference and one-day conference registrants.

WORKSHOPS
TTTC presents two two-day workshops on Thursday and Friday.

FRINGE TECHNICAL MEETINGS
TTTC committees and standards working groups.

TABLE OF CONTENTS

DAILY EXHIBIT HOURS

Tuesday	10:30 a.m. – 5:30 p.m.
Wednesday	9:30 a.m. – 4:30 p.m.
Thursday	9:30 a.m. – 1:00 p.m.

Complimentary lunch
Tuesday, Wednesday and Thursday
in the exhibit hall for full- and one-day
ITC conference registrants.

Free exhibits entry every day
(Registration required - lunch not
included)

Corporate Supporters

Diamond

SIEMENS

Platinum

ADVANTEST SYNOPSYS Silicon to Software GALAXY Chroma

Gold

winbond We Deliver

Caliber Interconnect Solutions design and test for perfection

Silver

proteanTecs GOPEL electronics Enjoy Testing cadence

Sponsors

IEEE

IEEE
Philadelphia Section

IEEE COMPUTER SOCIETY

TUTORIALS	Sunday, September 25	8:30 a.m. – 4:30 p.m.
	Monday, September 26	8:30 a.m. – 4:30 p.m.

The Tutorials and Education Group of the IEEE Computer Society Test Technology Technical Council (TTTC) organizes a comprehensive set of Test Technology Educational Program (TTEP) tutorials. TTEP offers fundamental education and expert knowledge in state-of-the-art test technology topics and also the opportunity to earn official certification from IEEE TTTC under the TTEP program.
The following 12 half-day tutorials qualify for credit towards IEEE TTTC certification.

Tutorials are a half-day in length. **One-Day** tutorial registration fee is for two tutorials—a morning tutorial and afternoon tutorial, both on the same day, e.g., Tutorial 1 and Tutorial 4 on Sunday. You may register for up to four tutorials (two consecutive on Sunday and two consecutive on Monday).
All-Access Pass tutorial registration provides in-and-out access to all twelve tutorials over both days. For more information, inquire at the registration counter.
Room assignments are subject to change. Please see the digital monitors for the latest information.

Sunday 8:30 a.m. – 12:00 p.m.

TUTORIAL 1 Magic Kingdom Ballroom 1
Dependability and Testability of AI Hardware
F. Su, H. Stratigopoulos, Y. Makris

TUTORIAL 2 Magic Kingdom Ballroom 3
Early System Reliability Analysis for Cross-layer Soft Errors
A. Bosio, S. Di Carlo, A. Salvino

TUTORIAL 3 Magic Kingdom Ballroom 4
Device-Aware Test for Emerging Memories
S. Hamdioui

Sunday 1:00 p.m. – 4:30 p.m.

TUTORIAL 4 Magic Kingdom Ballroom 1
Computation in Memory: Technologies, Design, Test and Reliability
M. Tahoori

TUTORIAL 5 Magic Kingdom Ballroom 3
Mixed-Signal DFT and BIST: Trends, Principles and Solutions
S. Sunter

TUTORIAL 6 Grand Ballroom North B
Scan Test Escapes, New Fault Models, and the Effectiveness of Functional System Level Tests
A. Singh

Monday 8:30 a.m. – 12:00 p.m.

TUTORIAL 7 Magic Kingdom Ballroom 1
Silicon Lifecycle Management for Emerging SOCs
Y. Zorian, F. Massoudi

TUTORIAL 8 Magic Kingdom Ballroom 3
Testing and Monitoring of Die-2-Die Interconnects in 2.5D/3D IC
S.-Y. Huang

TUTORIAL 9 Grand Ballroom North B
Domain-Specific Machine Learning in Semiconductor Test
L.-C. Wang

Monday 1:00 p.m. – 4:30 p.m.

TUTORIAL 10 Magic Kingdom Ballroom 1
Automotive Safety, Reliability and Test Solutions
R. Mariani, Y. Zorian

TUTORIAL 11 Magic Kingdom Ballroom 3
SoC Security Verification
M. Tahoori, F. Farahmandi

TUTORIAL 12 Grand Ballroom North B
Advances in Defect-Oriented Testing
A. Singh, A. Glowatz

Tutorial attendees receive study material, breaks and lunches on the days attended. Tutorial registration, coffee and pastry are available at 7:30 a.m. on Sunday and Monday. Lunch is served from 12:00 p.m. to 1:00 p.m.

Table of Contents

PANEL	Monday, September 26	4:30 p.m. – 6:00 p.m.

PANEL 1 **Magic Kingdom Ballroom 1 & 4**

An Industry-wide Dialog on Chiplets and Heterogeneous Integration

Moderator: Phil Nigh

Three short presentations will be followed by a dialog with the audience. The goal: to gather feedback on the HR roadmap projections and about current and future test standards. .

Panelists: *Jeff Rearick* (AMD) on chiplet trends and drivers
Yervant Zorian, Synopsys on UCIe
Ken Butler (Advantest) on HIR

Post-panel reception follows 6:00 p.m. – 7:30 p.m.

Following this panel on Monday afternoon, stick around for a reception to carry on the lively discussion. Meet us at the Adventure Lawn for some networking over libations and hors d'oeuvres.

Tomorrow (Tuesday)

Continental breakfast: 8:00 a.m.
Plenary: 9:00 a.m.
Exhibits open: 10:30 a.m. – 5:30 p.m.
Corporate forum: 11:30 a.m.
Exhibit hall lunch: 12:00 p.m.
Technical sessions: 2:00 p.m.
ITC Welcome Reception: 6:00 p.m. – 8:00 p.m.

ITC 2022 PROCEEDINGS DISTRIBUTION

ITC Proceedings Are Delivered Electronically

All ITC full-conference and one-day attendees, including students, will receive access to the 2022 ITC online proceedings free of charge.
.

Preregistered Full-Conference Attendees
All preregistered full-conference attendees should have received an email containing a proceedings download link a few days before the conference. The ITC 2022 technical presentations will be available at the Underline site for ITC. Information on how to access them will be provided to all registrants before the conference.

Onsite Full-Conference and One-Day Attendees
Full-conference and one-day attendees registering onsite will receive the links at the time of registration.

.

SUNDAY, SEPTEMBER 25 – HALF-DAY TUTORIALS			
8:30 a.m. – 12:00 p.m.	Tutorial 1 Dependability and Testability of AI Hardware	Tutorial 2 Early System Reliability Analysis for Cross-layer Soft Errors	Tutorial 3 Device-Aware Test for Emerging Memories
1:00 p.m. – 4:30 p.m.	Tutorial 4 Computation in memory: Technologies, Design, Test and Reliability	Tutorial 5 Mixed-Signal DFT and BIST: Trends, Principles and Solutions	Tutorial 6 Scan Test Escapes, New Fault Models, and the Effectiveness of Functional System Level Tests
MONDAY, SEPTEMBER 26 – HALF-DAY TUTORIALS			
8:30 a.m. – 12:00 p.m.	Tutorial 7 Silicon Lifecycle Management for Emerging SOCs	Tutorial 8 Testing and Monitoring of Die-2-Die interconnects in 2.5D/3D IC	Tutorial 9 Domain-Specific Machine Learning in Semiconductor Test
1:00 p.m. – 4:30 p.m.	Tutorial 10 Automotive Safety, Reliability and Test Solutions	Tutorial 11 SoC Security Verification	Tutorial 12 Advances in Defect-Oriented Testing
4:30 p.m. – 6:00 p.m.	Panel 1 - **An Industry-wide Dialog on Chiplets and Heterogeneous Integration**		

TUESDAY, SEPTEMBER 27 – TECHNICAL SESSIONS					
9:00 a.m. – 10:30 a.m.	**Plenary** – **Opening Session Keynote:** Make Computing Count: Some Grand Opportunities for Testing, *Parthasarathy Ranganathan*, Google				
10:30 a.m. – 5:30 p.m.	Exhibits				
11:00 a.m. – 12:00 p.m.	Diamond Supporter Presentation				
12:00 p.m. – 2:00 p.m.	Lunch and Corporate Forum				
2:00 p.m. – 3:30 p.m.	Session A1 New Frontiers in Fault Modeling	Session B1 Innovation and Machine Learning I	Session C1 Diagnosis and Debug	Session D1 TTTC McCluskey PhD Competition	Session E1 Special Session Dedicated to the Memory T. W. Williams, W. Maly and D. Pradhan
3:30 p.m. – 4:00 p.m.	Coffee Break				
4:00 p.m. – 5:30 p.m.	Session A2 Panel 2 Are Last Century's Test Techniques Suitable for 21st Century Silent Errors?	Session B2 Innovation with Machine Learning II	Session C2 New Frontiers in Test Content Optimization	Session D2 Test of HW Accelerators I	Session E2 Special Session: Experiences in Silicon Lifecycle Management
6:00 p.m. - 8:00 p.m.	ITC Welcome Reception – Adventure Lawn				

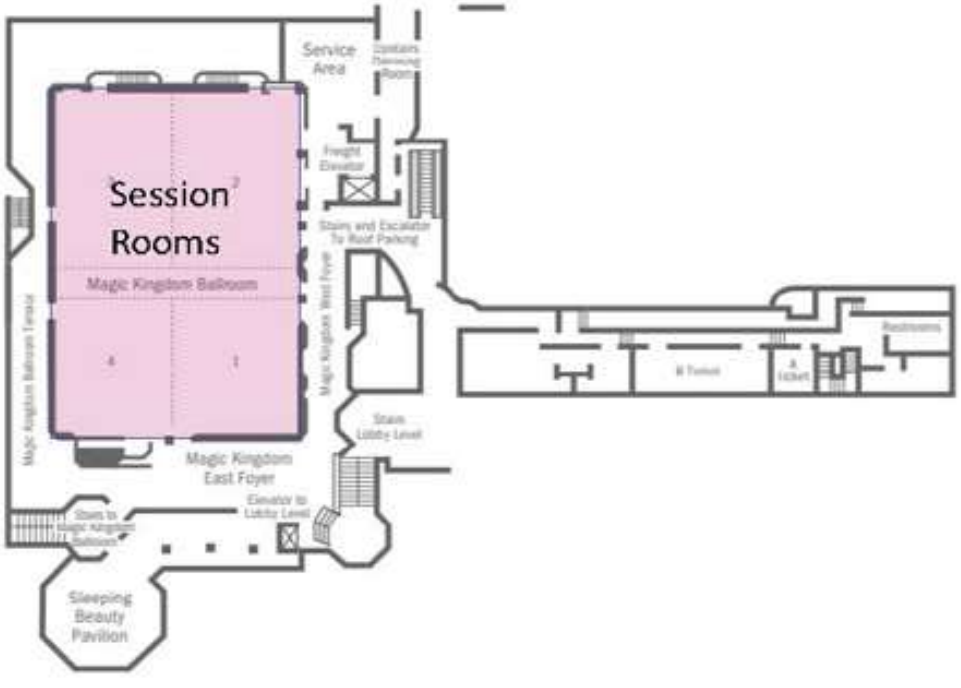
WEDNESDAY, SEPTEMBER 28 – TECHNICAL SESSIONS					
9:00 a.m. – 10:30 a.m.	**Plenary Session** **Keynote:** The Future of High-Performance Computing Beyond Moore's Law, *John Shalf,* Lawrence Berkeley National Labs **Visionary Talk**: Ultra Low-Power AI Accelerators for AIoT, *Tim Cheng,* The Hong Kong University of Science and Technology				
9:30 a.m. – 4:30 p.m.	Exhibits				
10:30 a.m. – 11:00 a.m.	Coffee Break and Corporate Forum				
11:00 a.m.– 12:30 p.m.	Session A3 Hardware Security I	Session B3 Latest on Wafer Map Analytics	Session C3 Memory Test/Diagnosis	Session D3 Special Session on Compute-In-Memory	Session E3 Industrial Practices I
12:30 p.m. – 2:30 p.m.	Lunch, Posters and Corporate Forum				
2:30 p.m. – 4:00 p.m	Session A4 Hardware Security II	Session B4 Test of HW Accelerators II	Session C4 Memory Test/Repair	Session D4 Automotive I	Session E4 Industrial Practices II
4:00 p.m. – 4:30 p.m.	Coffee Break				
4:30 p.m. – 6:00 p.m.	Session A5 Special Session on HW Security Certification	Session B5 Analog Testing	Session C5 Panel 3: Performing RAS in Today's Mission Critical Systems	Session D5 Automotive: Special Session on High-Power Electronics	Session E5 Analog Test, Diagnosis, Test Cost, All-In-One

Table of Contents

THURSDAY, SEPTEMBER 29 – TECHNICAL SESSIONS					
9:00 a.m. – 10:00 a.m.	**Plenary Session** **Keynote**: What Did We Learn in 120 Years of DFT and Test? *Grady Giles, Mike Bienek, & Tim Wood,* AMD				
9:30 a.m. – 1:00 p.m.	Exhibits				
10:00 a.m. – 10:30 a.m.	Coffee Break				
10:30 a.m.– 12:00 p.m.	Session A6 Special Session on Test of Quantum Circuits	Session B6 Scan-Based Learning and Diagnosis	Session C6 Special Session: Road to Chiplets: UCIe	Session D6 Automotive II	Session E6 Industrial Practices III
12:00 p.m. – 1:30 p.m.	Lunch				
1:30 p.m. – 3:00 p.m.	Session A7 Test Generation	Session B7 Low Power and Test	Session C7 Special Session: Design-for-Verification (DfV): A New Direction in Design Qualification	Session D7 Panel 4: Automotive Safety & Security Interoperability	Session E7 Special Session: Industrial Practices from ITC India
THURSDAY, SEPTEMBER 29 – WORKSHOPS					
4:00 p.m. – 6:30 p.m.	ART 2022: IEEE Automotive Reliability and Test & Safety Workshop 2022 Plenary1: Opening, Keynote		2nd IEEE Intl Workshop on Silicon Lifecycle Management (SLM) Plenary1: Opening, Keynote		
FRIDAY, SEPTEMBER 30 – WORKSHOPS					
8:00 a.m. – 4:00 p.m.	ART 2022: IEEE Automotive Reliability and Test & Safety Workshop 2022		2nd IEEE Intl Workshop on Silicon Lifecycle Management (SLM)		

ITC Floor Plan

DISNEYLAND, HOTEL—UPPER LEVEL



PLENARY 1	Tuesday, September 27	9:00 a.m. – 10:30

Disney Grand Ballroom

Opening Remarks

Teresa McLaurin, *ITC 2022 General Chair*

Keynote Address 1

Make Computing Count: Some Grand Opportunities for Testing

Parthasarathy Ranganathan
VP/technical Fellow, Google

This talk will discuss the trends shaping the future computing landscape, with a specific focus on the role of testing -- for correctness, agility, and performance -- and some grand challenges, and opportunities, for the field.

About the speaker: Partha Ranganathan is currently a VP, technical Fellow at Google where he is the area technical lead for hardware and datacenters, designing systems at scale.

ITC Paper Awards

Theresa McLaurin, *ITC 2021 Program Chair*

ITC Ned Kornfield Best Paper Award

Exploiting Application Tolerance for Functional Safety
P. V. Pillai, R. Parekhji, Texas Instruments, India; B. Amrutur, Indian Institute of Science

Honorable Mentions

A Fast and Low Cost Embedded Test Solution for CMOS Image Sensors
J. Lefevre,P. Debaud, STM Microelectronics; P. Girard, A. Virazel, LIRMM Imaging Division, DFT University of Montpellier

Improving Volume Diagnosis and Debug with Test Failure Clustering and Reorganization
M-T Wu, C-S Kuo, J. C-M Li, National Taiwan University; C. Nigh, G. Bhargava, Qualcomm

TTTC Awards

Yervant Zorian

TTTC Life Time Contribution Medal

ITC/TTTC G. Gordon Student Service Award

TTTC Bob Madge Innovation Award

ITC 2022 Technical Program Introduction

Kuen-Jong Lee, *ITC 2022 Program Chair*

Closing Remarks

T. McLaurin, *ITC 2022 General Chair*

Table of Contents

Exhibit Hall

The corporate forum allows you to stay on top of the latest commercial products in the semiconductor test industry and helps you understand how the innovations behind the products can add value to your workIn this interactive forum, ITC exhibitors and supporters will make presentations describing their company, its products and product roadmaps.. Typical presentations include case studies, best practices and testimonials.

11:00 a.m.–12:00 p.m.
Disney Grand Ballroom Center

Siemens
Diamond Supporter Event

1. DFT to In-Life monitoring for dependable electronic systems. A. Gupta, Siemens
2. Reducing Design Effort, Test Time And Power With SSN in AWS Custom Silicon, D. Trock, Amazon
3. Advancements in DFT automation for 2.5D / 3D IC era, V. Neerkundar, Siemens
4. Structural Deterministic Test in Silicon Lifecycle, J. Rajski, Siemens

12:00 p.m.–2:00 p.m.

Exhibit Hall

12:00 p.m. Synopsys

Test and Analytics: Enabling Silicon Lifecycle Management,
R. Ruiz, Synopsys

12:30 p.m. Advantest

Enabling Leading-Edge Technologies in an Exascale Era,
K. Schaub, Advantest

1:30 p.m. Chroma

Facing the Challenges in Automated Handling of Advanced IC Packaging,
J. Hauck, Chroma

1:45 p.m. Galaxy

Open Architecture and Democratized Data Systems: The Logical Evolution of Test Data Analytics,
D. King, Galaxy

SESSION A1 Magic Kingdom Ballroom 1

New Frontiers in Fault Modeling

S. Adham (Chair)

A1.1 PEPR: Pseudo-Exhaustive Physical Region Testing

W. Li, D. Duvalsaint, R. Blanton,* Carnegie Mellon University; *C. Nigh,* Qualcomm Technologies, Inc.; *S. Mitra,* Stanford University

A1.2 Error Model- A New Way of Doing Fault Simulation

N. Saxena, A. Lotfi*, NVIDIA

A1.3 Using Custom Fault Modelling to Improve Understanding of Silicon Failures

S. Kundu,* The University of Texas at Dallas; *G. Bhargava, L. Endrinal, L. Ranganathan,* Qualcomm Technologies Inc

SESSION B1 Magic Kingdom Ballroom 2

Innovation with Machine Learning I

K. Butler (Chair)

B1.1 DeepTPI: Test Point Insertion with Deep Reinforcement Learning

Z. Shi, M. Li, S. Khan, Q. Xu,* The Chinese University of Hong Kong; *L. Wang,* Huawei Technologies Co., Ltd.; *N. Wang, Y. Huang,* Hisilicon

B1.2 Efficient and Robust Resistive Open Defect Detection Based on Unsupervised Deep Learning

Y. Liao, Z. Najafi-Haghi, H-J. Wunderlich, B. Yang,* University of Stuttgart

B1.3 RCANet: Root Cause Analysis via Latent Variable Interaction Modeling for Yield Improvement

X. Zhang, E. Young,* The Chinese University of Hong Kong; *S. Hu, Z. Chen, S. Zhu, J. Hao,* Huawei Noahs Ark Lab; *P. Li, C. Chen, Y. Huang,* HiSilicon

* Presenter

SESSION C1 Magic Kingdom Ballroom 3

Diagnosis and Debug

S-Y Huang (Chair)

C1.1 Scaling Physically Aware Logic Diagnosis to Complex High Volume 7nm Server Processors
B. Nandakumar, S. Chillarige, M. Maheshwari,* Cadence Design Systems; *R. Redburn, J. Zimmerman, N. L'Esperance, E. Dziarcak,* IBM

C1.2 Diagnosing Double Faulty Chains through Failing Bit Separation
C-S. Kuo, J-M. Li, B-H. Hsieh,* National Taiwan University; *C. Nigh, M. Chern, G. Bhargava,* Qualcomm Technologies Inc

C1.3 Transient Fault Pruning for Effective Candidate Reduction in Functional Debugging
D-A. Yang, National Tsing Hua University, Department of Electrical Engineering; *J-J. Liou*,* National Tsing Hua University, Department of Electrical Engineering; *H. Chen,* MediaTek Inc., Computing and AI Technology Group

SESSION D1 Magic Kingdom Ballroom 4

TTTC PhD Thesis Competition - Final Round

M. Portolan (Chair)

D1.1 Next Generation Design For Testability, Debug and Reliability Using Formal Techniques
S. Huhn,* University of Bremen; *R. Drechsler,* University of Bremen, Germany

D1.2 Testing of Analog Circuits using Statistical and Machine Learning Techniques
S. Srimani, H. Rahaman,* Indian Institute of Engineering Science and Technology

D1.3 AI-Driven Assurance of Hardware IP against Reverse Engineering Attacks
P. Charaborty, S. Bhunia,* University of Florida

SESSION E1 Grand Ballroom South AB

Special Session Dedicated To The Memory Of Tom W. Williams, Wojciech Maly and Dhiraj Pradhan

Y. Zorian (Chair)

E1.1 Wojciech Maly Memorial
A. Meixner, IBM*; P. Nigh,* Broadcom

***E1.2* Tom W Williams Memorial**
R. Mercer; S. Mitra, Stanford

***E1.3* Dhiraj K Pradhan Memorial**
A. Singh, Auburn U; *S. Gupta*, USC

.

.

Table of Contents

SESSION A2 Magic Kingdom Ballroom 1

Panel: Are Last Century's Test Techniques Suitable for 21st Century Silent Errors?
S. Chakravarty, Intel; *S. Mitra*, Stanford (Organizers)
J. Rearick (Moderator)

Panelists:
R. Govindaraju, Google
H. Dixit, Meta
P. Bose, IBM
S. Chakravarty, Intel
S. Mitra, Stanford

SESSION B2 Magic Kingdom Ballroom 2

Innovation with Machine Learning II
H.-P. Wen (Chair)

B2.1 Neural Fault Analysis for SAT-based ATPG
J. Huang, Noah's Ark Lab, Huawei; *H-L. Zhen**, Noah's Ark Lab, Huawei; *N. Wang*, Hisilicon, Huawei; *H. Mao*, Noah's Ark Lab, Huawei; *M. Yuan*, Noah's Ark Lab, Huawei; *Y. Huang*, Hisilicon, Huawei

B2.2 Improving Test Quality of Memory Chips by a Decision Tree-Based Screening Method
*Y-C. Cheng**, *M-D. Shieh*, NCKU; *P-Y. Tan*, *C-W. Wu*, NTHU; *C-H. Chien-Hui Chuang*, *G. Liao*, TSMC

B2.3 Fault Resilience Techniques for Flash Memory of DNN Accelerators
*S-K. Lu**, *Y-S. Wu*, National Taiwan University of Science and Technology; *J-H. Hong*, National University of Kaohsiung; *K. Miyase*, Kyushu Institute of Technology

SESSION C2 Magic Kingdom Ballroom 2

New Frontiers in Test Content Optimization
P. Song (Chair)

C2.1 Automatic Structural Test Generation for Analog Circuits using Neural Twins
J. Talukdar, *A. Chaudhuri**, *K. Chakrabarty*, Duke University; *M. Bhattacharya*, Synopsys

C2.2 DEFCON: Defect Acceleration through Content Optimization
*S. Natarajan**, *A. Sathaye*, *C. Oak*, *N. Chaplot*, *S. Banerjee*, Intel Corporation

C2.3 Low Capture Power At-Speed Test with Local Hot Spot Analysis to Reduce Over-Test
*A. Srivastava**, *J. Abraham*, Qualcomm Inc

SESSION D2 Magic Kingdom Ballroom 4

Test of HW Accelerators I
K. Chakravadhanula (Chair)

D2.1 A Multi-level Approach to Evaluate the Impact of GPU Permanent Faults on CNN's Reliability
*J. Rodriguez Condia**, *J. Guerrero Balaguera*, *M. Sonza Reorda*, Politecnico di Torino; *F. Fernandes dos Santos*, Institut National de Recherche en Sciences et Technologies du Numérique (INRIA); *P. Rech*, University of Trento

D2.2 Accelerating RRAM Testing with Low-cost Computation-in-Memory based DFT
*A. Singh**, *M. Fieback*, *R. Bishnoi*, *F. Bradaić*, *A. Gebregiorgis*, *S. Hamdioui*, TU Delft; *R. Joshi*, IBM

D2.3 Compact Functional Test Generation for Memristive Deep Learning Implementations Using Approximate Gradient Ranking
S. Ahmed, Karlsruhe Institute Of Technology; *M. Tahoori**, Karlsruhe Institute of Technology (KIT), Faculty of Informatik

SESSION E2 Grand Ballroom South AB

Special Session: Experiences in Silicon Lifecycle Management
Y. Zorian (Organizer)
Swapnil Bahl (Chair)

E2.1 In-Field System Debug and Silicon Life Cycle Management of Compute Systems
S. Menon, R. Kuehnis, R. Kandula, Intel

E2.2 Sensor Aware Production Testing
F. Massoudi, A. Patel, K. Darbinian, Y. Zorian, Synopsys

E2.3 *Addressing System-Level Challenges for Power-On Self-Test*
R. Kumar Tiwari, S. Tandon, M. Singla, S. Patil, Qualcomm

ITC Welcome Reception **Tuesday, September 27** **6:00 p.m. – 8:00 p.m.**

Adventure Lawn

Join the party on Tuesday, September 27, from 6:30-8:30 PM. Reconnect with friends and colleagues for the first time in three years. Food and beverage for all registered attendees and exhibitors. The past two years we had to party virtually, now we can party for real.

Tomorrow (Wednesday)

Continental breakfast: 8:00 a.m.

Keynote and Visionary Talks: 9:00 a.m.

Technical sessions: 11:00 a.m.

Exhibits open: 9:30 a.m. – 4:30 p.m.

.

Lunch, Poster Session and Corporate Forum: 12:30 a.m.

Technical sessions: 2:30 p.m.

Keynote Address2 **Disney Grand Ballroom Center**

The Future of High-Performance Computing Beyond Moore's Law
John Shalf
Lawrence Berkeley National Labs
J. Rearick (Chair)

There are a number of developments that will change how we will compute in 10 years: the foreseeable end of Moore's law will lead to the exploration of new architectures and the introduction of new technologies in HPC; the rapid progress in machine learning in the last decade has led to a refocus of HPC towards large scale data analysis and machine learning; the feasibility of quantum computing has led to the introduction of new paradigms for scientific computing; meanwhile 30 billion IOT devices will push advances in energy efficient computing and bring an avalanche of data.

About the speaker: John Shalf is Department Head for Computer Science at Lawrence Berkeley National Laboratory, and recently was deputy director of Hardware Technology for the DOE Exascale Computing Project.

Visionary Talk
Ultra Low-Power AI Accelerators for AIoT – Compute-in-memory, Co-Design, and Heterogeneous Integration
Tim Cheng
The Hong Kong University of Science and Technology
K-J Lee, (Chair)

We will give an overview of the objectives and some recent progress in designing ultra-low-power AI accelerators for supporting a wide range of AIoT devices with powerful embedded intelligence and test.

About the speaker: Tim Cheng is currently Vice-President for Research and Development at Hong Kong University of Science and Technology (HKUST) and Chair Professor jointly in the Departments of ECE and CSE., music analysis/retrieval, image classification, medical/healthcare data analytics, and FinTech.

SESSION A3 Magic Kingdom Ballroom 1

Hardware Security I

J. Dworak (Chair)

A3.1 RTL-FSMx: Fast and Accurate Finite State Machine Extraction at the RTL for Security Applications
R. Kibria, M. Rahman, F. Farahmandi, M. Tehranipoor,* University of Florida

A3.2 TAMED: Transitional Approaches for LFI Resilient State Machine Encoding
M. Choudhury, M. Gao, S. Tajik, D. Forte,* University of Florida

A3.3 Reliability Study of 14 nm Scan Chains and Its Application to Hardware Security
F. Stellari, P. Song,* IBM

SESSION B3 Magic Kingdom Ballroom 2

Latest on Wafer Map Analytics

J. Li (Chair)

B3.1 Language Driven Analytics for Failure Pattern Feedforward and Feedback
M. Yang, Y. Zeng, L-C. Wang,* University of California Santa Barbara

B3.2 Wafer Map Defect Classification Based on the Fusion of Pattern and Pixel Information
Y. Liao, P. Genssler, H. Amrouch, B. Yang,* University of Stuttgart; *R. Latty,* Advantest Europe GmbH

B3.3 WXAI: Wafer Defect Pattern Classification with Explainable Rule Based Decision Tree Methodology
K-C. Cheng, A-A. Huang, C-S. Lee, L-Y. Chen, P-Y. Liao, N-Y. Tsai,* NXP Semiconductors Taiwan Ltd.; *K-M. Li,* National Sun Yat-Sen University; *S-J. Wang,* National Chung Hsing University

B3.4 Yield-Enhanced Probing Cleaning with AI-Driven Image and Signal Integrity Pattern Recognition for Wafer Test
N. Sinhababu, S, J. Wang,* NXP Semiconductors Taiwan Ltd.; *K-M. Li,* National Sun Yat-Sen University; *J-D. Li, S-J. Wang,* National Chung Hsing University

SESSION C3 Magic Kingdom Ballroom 3

Memory Test/Diagnosis

S-K Lu (Chair)

C3.1 Fault Diagnosis for Resistive Random- Access Memory and Monolithic Inter-tier Vias in Monolithic 3D Integration
S-C. Hung, A. Chaudhuri, K. Chakrabarty,* Duke University; *S. Banerjee,* Intel Corporation

C3.2 Fault Modeling and Testing of Memristor-Based Spiking Neural Networks
K-W. Hou, H-H. Cheng, C. Tung,* National Tsing Hua University; *C-W. Wu,* NTHU; *J-M. Lu,* Industrial Technology Research Institute

C3.3 Fault-coverage Maximizing March Tests for Memory Testing
R. Feng, Y. Lin, Y. Lou, L. Gao, V. Gera, B. Li, V. Chowdary Nekkanti, A. Rajendra Pharande, K. Sheth, M. Thommondru, G. Ye, University of Southern California; *S. Gupta*,* Purdue University

C3.4 Enhanced Data Pattern to Detect Defects in Flash Memory Address Decoder
J. Soh, C. He,* NXP Semiconductors

SESSION D3 Magic Kingdom Ballroom 4

Special Session on In-Memory Computing Design and Test Challenges
S. Adham, TSMC; *S. Hamdioui*, Delft, University *(Organizers)*
A. Adham (Chair)

D3.1 In-Memory Computing: History, Overview, Current and Future Directions
N. Shanhbag,* Univ. of Illinois

D3.2 Testing Computation-in-Memory Architectures Based on Memristive Devices
S. Hamdioui,* Delft, University

D3.3 Fully Digital Compute In Memory Design and Test challenges
*S. Adham**, TSMC

* Presenter

SESSION E3 Grand Ballroom South AB
Industrial Practices I
P. Nigh (Chair)

E3.1 Application of Sampling in Industrial Analog Defect Simulation
M. Bhattacharya, B. Solignac, M. Durr,* Synopsys

E3.2 Challenges for High Volume Testing of Embedded IO Interfaces in Disaggregated Microprocessor Products
E. Garita-Rodriguez, R. Rimolo-Donadio, R. Zamora-Salazar,* Intel

E3.3 New R&R Methodology in Semiconductor Manufacturing Electrical Testing
A. Pagani, F. Brembilla,* STMicroelectronics

Exhibit Hall

PO.1 Neural Machine Translation for Test Language
S Go, SungKyunKwan University, Samsung Electronics

PO.2 Compositive Framework for Wafer Pattern Recognition with Confidence Relabeling Technique
L-Y Chen, Y-A Huang, C-S Lee, C-C Cheng, Y-Y Liao, L Chou J. Elwell, PNXP Semiconductors*; S-M Li,* National Sun Yat-Sen University*; S-J Wang,* National Chung Hsing University

PO.4 Teradyne's PortBridge Software Expedites Silicon Bring-Up, Debug, Production Readiness and Foundry Feedback
*R. Fanning,*Teradyne*; S. Molavi,* Broadcom

PO.5 Bridging Repairability Gaps in Shared Bus Architecture with Shared Physical Memory Implementation
W. Pradeep, N. Karkare; Google

PO.6 Design-for-Diagnosis for Multiple Defects per Chain
E. Gizdarski, Y. Kanzawa, Synopsys

PO.7 Roadblocks and Strategy to the Reuse of Test Solutions for Analog and Mixed-Signal Blocks
P. Bauwens, R. Vanhooren, A. Coyette, W. Dobbelaere, onsemi; G. Gielen, N. Xama, J. Gomez, KU Leuve

PO.8 Leveraging Existing High Speed Functional Serial Interfaces for Testing & Monitoring Silicon Throughout the Entire Lifecycle
R. Allen, A. Patel, Synopsys; K. Hilliges, Advantest; *B. Tully, A. Pandey,* Amazon

PO.9 Chiplet Level Test Parallelization for 3D Stacking Products
A. Margulis, T. Payakapan, J. Yuan, N.l Patel, A. Loh, AMD

PO.10 Pre-Analysis for ATPG Pattern Failures
D. Appello, D. Petrali, V. Tancorre, STMicroelectronics*; G. Chan, R. Dokken,* Roguevation

PO.11 Accelerating Design Cycle with DFT and Test Coverage Analysis at RTL
M. Arneson, Micron Technology*; R. Singhal, S. Nanduru,* Synopsys

PO.12 Prediction of Total Jitter using Machine Learning for LVDS Output Characterization
P. L. Lee, Intel

PO.13 Ehanced Jitter Reduction for Multi-GHz ATE
D. Keezer, Eastern Institute for Advanced Study*; D. Minier,* Boreas Technologies

PO.14 Deploying Real-Time Machine Learning Applications with Deep Data at Test
M. Hutner, A. Burlak, A. Mittall, proteanTecs

PO.15 HBM3 Test/Debug Solution Supporting PHY-Mastered Interface of HBMPHY
H. Son, Y. Lim, D. Han, Samsung Foundry

PO.16 Enabling a Low Cost and High Quality Scan Test Methodology in 16nm FinFet Automotive Products
S. Traynor, J. T. Ng, R. Chen., NXP Semiconductor

PO.17 Ultra-Fast and Secure 5G Digital Pre-Distortion with ACS Edge
D. Belkin, O. Olansky, Intel*; Y. Chen, K. Butler, K. Schaub,* Advantest

PO.18 **IR-Drop Improvement with Packet-Based Scan**
J. Reynick, Siemens EDA*; S. Alampally.,* Broadcom

PO.19 Investigation of Jitter Spur Impact on Eye Width Margin
O. Choong, W. C. Liew, Intel

PO.20 Improving Engineering Efficiency & Time to Market Through Multi-Variable Characterization
D. King, Galaxy Semiconductor

PO.21 Re-targeting Block-Level Patterns Using Top-Level On-Chip Clock Controller (OCC) --- An Industrial Case Study
Z. Zhong, S. Biswas, A. Wangoo, M. Bhattarai; Marvell Semiconductor Inc*; A. Gangwar,* Synopsys

PO.22 Identical HW and SW for producton test and lab validation of modules
F. Haas, A. Matiz, ams-OSRAM

PO.23 Cell-Aware Test integration towards achieving 0 DPPB on automotive designs
N. K, S. Ramesh, R. Kaistha, J. K. Loh, G. S Clark, C. Ling, NXP Semiconductors

PO.24 A Novel Shift-left Method in Reducing Networking ASIC Customer Field DPM
K. A. Chuah, T. H. H. Tan, C. C. Tan, Intel

PO.25 Lcpll DTR: Recovering Yield Loss with Fusing and Graphics Driver
N. Wang-Lee, J. Abbas, K. L. Ng, H. Zhao, Y. Park, Intel

PO.26 An Application of Spatially Resolved Netlists to Graphical Error Detection
N. Taylor, J. Delozier, T. McDonley, K. Liszewski, B. Hayden, A. Kimura, Battelle Memorial Institute

PO.27 Low Cost, At-Speed Validation of I3C Target Design
P. Bansal, P. Bal, A. Kumari, STMicroelectronics

PO.28 ATE Integration of High Performance, High Data Rate 3rd Party Instruments
T. Lyons, Teradyne

PO.29 A Novel DFT [Design for Test] Clock Gating Technique to Reduce Power Consumption
A. Gangwar, F. Shukla, Synopsys; *S. Murthy, P. Policke,* Qualcomm

PO.31 Test Manufacturing Breakthroughs To Maximize Total Sellable Yield in 5G Network ASIC.
S. E. Wong, Intel

PO.32 A Breakthrough Manufacturing Solution - Array Erratic Fluctuation Predictive through Machine Learning Methods
N. H. Chun, T. Aik, Intel

PO.33 Advanced Core Wrapping for Power, Early Test Coverage and Automation
A. Gangwar, F. Shukla, K. Bachu, Synopsys

PO.34 Speedup Logic Diagnosis with Static Layout Data
R. Guo, Synopsys

PO.35 Design for test (DFT) Considerations when Designing Tile-based/abutted Physical Blocks
V. Neerkundar, Siemens

PO.36 Improving System Level Screening Efficiency Through Negative Voltage Margining
L.D. Rojas, J. Rodriguez, D. Wilhelmi, D. Lerner, Intel

PO.37 Built-In Self-Test architecture enabling diagnosis for massive Embedded Memory banks in large SoCs
G. Insinga, P. Bernardi, G. Paganini, A. Guerriero, Politecnico di Torino; *W. Mischo, R. Ullmann, M. Coppetta, G. Carnevale,* Infineon Technologies

10:30 a.m.–11:00 a.m.

Exhibit Hall

10:30 a.m. UNITES Systems

Testing SiC and GaN discrete semiconductors,
O. Betak, UNITES Systems

10:40 a.m. Xallent, Inc

Thin Films Testing Up to 300X Faster,
Kwame Amponsah, Xallent

10:50 a.m. yieldHUB

Revolutionize your yield management, C. S. Moore, yieldHub

1:30 p.m.–3:00 p.m.

Exhibit Hall

1:30 p.m. Chroma

High Multisite Testing for Hi Fidelity True Wireless Stereo (TWS) Devices,
E. Lin, Chroma

1:45 p.m. DR Yield

YieldWatchDog Solution for AI Test Data Analytics,
K. Tropper, DR Yield

2:00 p.m. Caliber Interconnect Solutions

Value Proposition - Caliber Interconnect Solutions,
M. Berry, Caliber

2:15 p.m. Roos Instruments, Inc.

Roos Cassini: Continuous Coverage to 110GHz,
M. Roos, Roos

.

SESSION A4 Magic Kingdom Ballroom 1

Hardware Security II

P. Song (Chair)

A4.1 Modeling Challenge Covariances and Design Dependency for Efficient Attacks on Strong PUFs
H. Wang, W. Liu, H. Jin, Y. Chen, W. Cai,* Huazhong University of Science and Technology

A4.2 ADWIL: A Zero-Overhead Analog Device Watermarking Using Inherent IP Features
U. Das, M. Muttaki, M. Tehranipoor, F. Farahmandi,* University of Florida

A4.3 Circuit-to-Circuit Attacks in SoCs via Trojan-Infected IEEE 1687 Test Infrastructure
M. Portolan,* Univ Grenoble Alpes, CNRS; *A. Pavlidis, H. Stratigopoulos,* Sorbonne Université LIP6; *G. Di Natale,* CNRS; *E. Faehn,* ST Microelectronics

A4.4 Hardware Root of Trust for SSN-based DFT Ecosystems
J. Tyszer, B. Wlodarczak, Poznan University of Technology; *J. Rajski*, M. Trawka,* Siemens Digital Industries Software

SESSION B4 Magic Kingdom Ballroom 2

Test of HW Accelerators II

S. Gupta (Chair)

B4.1 Functional In-Field Self-Test for Deep Learning Accelerators in Automotive Applications
T. Uezono, Hitachi; *Y. He*, Y. Li,* University of Chicago

B4.2 Defect-Directed Stress Testing Based on Inline Inspection Results
C. He, P. Grosch, O. Anilturk, J. Witowski, C. Ford, R. Kalyan,* NXP Semiconductors; *J. Robinson, D. Price, J. Rathert, B. Saville,* KLA Corporation

B4.3 The Impact of On-chip Training to Adversarial Attacks in Memristive Crossbar Arrays
B. Paudel, S. Tragoudas,* Southern Illinois University, Carbondale

B4.4 RIBoNN: Designing Robust In-Memory Binary Neural Network Accelerators
S. Kundu, K. Basu,* The University of Texas at Dallas; *A. Malhotra, S. Gupta,* Purdue University; *A. Raha,* Intel Corporation

SESSION C4 Magic Kingdom Ballroom 3

Memory Test/Repair

J. Yun (Chair)

C4.1 Configurable BISR Chain For Fast Repair Data Loading
W. Zou, B. Nadeau-Dostie,* Siemens EDA

C4.2 Efficient Built-In Self-Repair Techniques with Fine-Grained Redundancy Mechanisms for NAND Flash Memories
S-K. Lu, S-C. Tseng,* National Taiwan University of Science and Technology; *K. Miyase,* Kyushu Institute of Technology

C4.3 Analyzing the Electromigration Challenges of Computation in Resistive Memories
M. Mayahinia, Karlsruhe Institute of Technology (KIT); *M. Tahoori*,* Karlsruhe Institute of Technology (KIT), Faculty of Informatik; *M. Perumkunnil, K. Croes, F. Catthoor,* IMEC

C4.4 DFT-Enhanced Test Scheme for Spin-Transfer-Torque (STT) MRAMs
Z-W. Pan, J-F. Li,* National Central University

SESSION D4 Magic Kingdom Ballroom 4

Automotive I

P. Wohl (Chair)

D4.1 An innovative Strategy to Quickly Grade Functional Test Programs
P. Bernardi, A. Francesco, S. Quer, L. Cardone, A. Calabrese, D. Piumatti, A. Niccoletti*, Politecnico di Torino; *D. Appello, V. Tancorre, R. Ugioli*, STMicroelectronics

D4.2 A Practical Online Error Detection Method for Functional Safety Using Three-Site Implications
*K. Ioki**, ROHM Co., Ltd.; *Y. Kai, K. Miyase, S. Kajihara*, Kyushu Institute of Technology

D4.3 PPA Optimization of Testpoints in Automotive Designs
B. Foutz, S. Singhal, P. Rai, K. Chakravadhanula, V. Chickermane, B. Nandakumar, S. Chillarige, C. Papameletis, S. Ravichandran*, Cadence Design Systems

SESSION E4 Grand Ballroom South AB

Industrial Practices II

C-W Wu (Chair)

E4.1 Accurate Failure Rate Prediction Based on Gaussian Process Using WAT Data
M. Eiki, M. Kajiyama, T. Nakamura*, Sony Semiconductor Manufacturing; *M. Shintani*, Kyoto Institute of Technology; *M. Inoue*, Nara Institute of Science and Technology

E4.2 4.5Gsps MIPI D-PHY Receiver Circuit for Automatic Test Equipment
S. Lee, C. Park, M. Kang, J. Won, H. Ryu, J. Choi, B. Yim*, Samsung Electronics

E4.3 Optimization of Tests for Managing Silicon Defects in Data Centers
D. Lerner, B. Inkley, S. Sahasrabudhe, E. Hansen, A. Van De Ven*, Intel Corporation

E4.4 Improving Structural Coverage of Functional Tests with Checkpoint Signature Computation
B. Niewenhuis, D. Varadarajan*, Texas Instruments

E4.5 Zero Trust Approach to IC Manufacturing and Testing
*B. Buras**, Advantest; *C. Xanthopoulos, J. Kim, K. Butler*, Advantest America Inc

E4.6 Virtual Prototyping: Closing the Digital Gap between Product Requirements and Post-Si Verification & Validation
T. Nirmaier, M. Harrant, M. Huppmann, G. Pelz*, Infineon Technologies

* Presenter

Table of Contents

SESSION A5 Magic Kingdom Ballroom 1

Special Session on HW Security Certification

T-Y Chan (Chair)

A5.1 Latest Cybersecurity Regulations, Certifications and Labeling Trends
*R. Menda-Shabat**, Winbond

A5.2 GlobalPlatform: 20 years of Security Evaluation on Secure Components,
G. Bernabeu,* GlobalPlatform

A5.3 Hardware Security in IoT Platforms and Certification
T.-Y. Chan,* Winbond

SESSION B5 Magic Kingdom Ballroom 2

Analog Testing

H. M. von Staudt (Chair)

B5.1 ML-Assisted Bug Emulation Experiments for Post-Silicon Multi-Debug of AMS Circuits
J-Y. Lei, A. Chatterjee,* Georgia Institute of Technology

B5.2 A Path Selection Flow for Functional Path Ring Oscillators using Physical Design Data
T. Kilian,* Infineon Technologies AG / Technical University of Munich; *M. Hanel, U. Schlichtmann,* Technical University of Munich; *D. Tille,* Infineon Technologies AG; *M. Huch,* Infineon Technology AG

B5.3 IEEE P1687.1: Extending the Network Boundaries for Test
M. Laisne, H. von Staudt, Dialog Semiconductor - a Renesas Company; *A. Crouch,* Amida Technology Solutions, Inc.; *M. Portolan,* Univ Grenoble Alpes, CNRS; *M. Keim*,* Siemens Digital Industries Software; *B. Van Treuren,* VT Enterprises Consulting Services; *J. Rearick,* Advanced Micro Devices; *S. Zuo,* Tailored Management

SESSION C5 Magic Kingdom Ballroom 3 PANEL 3

Performing RAS in Today's Mission Critical Systems

Y. Zorian (Organizer)
P. Benardi (Moderator)

Panelists:
R. Kinger, Google
N. Saxena, Nvidia
H. Dixit, Meta
Y. Zorian, Synopsys
D. Gizopoulos, Univ of Athens
C. Liu, Alibaba

SESSION D5 Magic Kingdom Ballroom 4

Automotive: Special Session on High-Power Electronics

S.-Y. Huang, National Tsing Hua University (Organizer, Chair)

D5.1 The Importance and Demand Market of SiC Substrate Defect Testing,
W-C Chang,* Industrial Technology Research Institute

D5.2 Validation of SPICE Models for Commercial SiC MOSFETs
H-Y Teng,* Industrial Technology Research Institute

D5.3 Practice Design Experiences on a Multi-Voltage-Level Motor Driver System using a Power Inverter
C-C Chiu,* Industrial Technology Research Institute

SESSION E5 Grand Ballroom South AB

Analog Test, Diagnosis, Test Cost, All-In-One

A. Singh (Chair)

E5.1 Efficient Low Cost Alternative Testing of Analog Crossbar Arrays for Deep Neural Networks
K. Ma, A. Saha, C. Amarnath,A. Chatterjee,* Georgia Institute of Technology

E5.2 Low-Cost High Accuracy Stimulus Generator for On-chip Spectral Testing
K. Bhatheja, S. Chaganti, D. Chen*, Iowa State University*; X. Jin, C. Dao, J. Ren, A. Kumar, D. Correa, M. Lehrmann, T. Rodriguez, E. Kingham, J. Knight. A. Dobbin, S. Herrin, D. Garrity,* NXP Semiconductors

E5.3 Optimal Order Polynomial Transformation for Calibrating Systematic Errors in Multisite Testing
P. Farayola, I. Bruce, D. Chen, Iowa State University*; S. Chaganti*, A. Sheikh, S. Ravi,* Texas Instruments

E5.4 Transforming an n-Detection Test Set into a Test Set for a Variety of Fault Models
I. Pomeranz,* Purdue University

E5.5 Improvements in the Automated IC Socket Pin Defect Detection
V. Thangamariappan, N. Agrawal, C. C Xanthopoulos, J. Kim, I. Leventhal, K. Butler*, Advantest America*; J. Xiao*, **Essai**

E5.6 GreyConE: Greybox Fuzzing + Concolic Execution Guided Test Generation for High Level Designs
M. Debnath, S. Sur-Kolay,* Indian Statistical Institute; *A Chowdhury*, New York University; *D. Saha,* University of Calcutta

Tomorrow (Thursday)

Continental breakfast: 8:00 a.m.

Keynote Talk: 9:00 a.m.

Technical sessions: 10:30 a.m.

Exhibits open: 10:00 a.m. – 1:00 p.m.

Lunch: 12:00 p.m.

Technical sessions: 1:30 p.m.

Workshops: 3:30 p.m.

Fill in your Exhibit Hall Passport for Prizes

PLENARY 3 — Thursday, September 29 — 9:00 a.m.– 10:00

Keynote Address 3 — **Disney Grand Ballroom Center**

What Did We Learn in 120 years of DFT and Test?

Grady Giles, Mike Bienek, & Tim Wood
AMD
Y. Zorian (Chair)

This interview-style discussion will feature three industry veterans whose careers have followed (and propelled) the growth in our field. We plan to reflect on how our industry has evolved, how this conference has reflected and driven that evolution, what lessons were learned, and what we can expect (and make happen) next. Along the way, we'll share some anecdotes, tell some stories, brag about some accomplishments, and humbly give some advice on things we found out the hard way (so that you don't have to).

.

About the speakers: Grady Giles, Mike Bienek, and Tim Wood are all members of the DFX team at AMD, with a combined 120+ years of experience in the industry.

Also in this session – announcement of the winner of the TTTC PhD Thesis Competition

TECHNICAL SESSIONS — Thursday, September 29 — 10:30 a.m. – 12:00 p.m.

SESSION A6 Magic Kingdom Ballroom 1

Special Session on Test of Quantum Circuits
J. Li, (Chair)

A6.1 Qubit fluctuations in quantum systems
M. Carroll,* IBM

A6.2 Introduction to Quantum Circuit Testing (from Test Engineer's Perspective)
*J. Li**, National Taiwan University

SESSION B6 Magic Kingdom Ballroom 2

Scan-Based Learning and Diagnosis
W-T Cheng (Chair)

B6.1 Scan-Based Test Chip Design with XOR-based C-testable Functional Blocks
Y-F. Chen, Dept. EE, National Cheng Kung University; *D-Y. Kang*,* Dept. EE, National Cheng Kung University; *K-J. Lee,* Dept. EE, National Cheng Kung University

B6.2 Industry Evaluation of Reversible Scan Chain Diagnosis
S. Urban, J. Janicki, M. Sharma, W-T. Cheng, Siemens EDA; *M. Parley, K. Chung, S. Nicholson, S. Mittal*,* Qualcomm

B6.3 A Comprehensive Learning-Based Flow for Cell-Aware Model Generation
P. d'Hondt,* LIRMM / STMicroelectronics; *A. Ladhar,* STMicroelectronics; *P. Girard, A. Virazel,* LIRMM

B6.4 Runtime Fault Diagnostics for GPU Tensor Cores
S. Hukerikar, N. Saxena,* NVIDIA

SESSION C6 Magic Kingdom Ballroom 3

Special Session: Road to Chiplets: UCIe
Y. Zorian (Chair)
Presenters: *D. D. Sharma*, Intel, *Y. Zorian,* Synopsys. *K-D Hillinges, M. Braun,* Advantest

* Presenter

SESSION D6 Magic Kingdom Ballroom 4
Automotive II
C. He **(Chair)**

D6.1 Unsupervised Learning-based Early Anomaly Detection in AMS Circuits of Automotive SoCs
A. Arunachalam, A. Kizhakkayil,* University of Texas at Dallas; *S. Kundu, K. Basu,* The University of Texas at Dallas; *A. Raha, S. Banerjee, F. Su,* Intel Corporation; *X. Jin,* NXP Semiconductors

D6.2 Just-Enough Stress Test for Infant-Mortality Screening Using Speed Binning
C-L. Tsai, S-Y. Huang,* National Tsing Hua University

D6.3 Existence of Single-Event Double-Node Upsets (SEDU) in Radiation-Hardened Latches for Sub-65 nm CMOS Technologies
M-H. Hsiao, P-T. Wang, C-W. Liang, H-P. Wen,* National Yang Ming Chiao Tung University

SESSION E6 Grand Ballroom South AB
Industrial Practices III
K. Peng (Chair)

E6.1 Probeless DfT Concept for Testing 20k I/Os of an Automotive Micro-LED Headlamp Driver IC
H. von Staudt,* Dialog Semiconductor - a Renesas Company; *L. Elnawawy,* Dialog Semiconductor, A Renesas Company; *S. Wang,* Dialog Semiconductor, A Renesas Company; *L. Ping,* Dialog Semiconductor, A Renesas Company; *J. Choi,* Samsung Electronics

E6.2 Reusing IEEE 1687-Compatible Instruments and Sub-Networks over a System Bus
F. Ghani Zadegan, Z. Zhang, K. Petersén, Ericsson; *E. Larsson*,* Lund University

E6.3 Multi-die Parallel Test Fabric for Scalability and Pattern Reusability
A. Sinha, Y. Cho, J. Easter, M. V. Leiva Rojas,* Intel

TECHNICAL SESSIONS Thursday, September 29 1:30 p.m. – 3:00 p.m.

SESSION A7 Magic Kingdom Ballroom 1
Test Generation
S-K Lu (Chair)

A7.1 Compression-Aware ATPG
X. Wang,* University of Chinese Academy of Sciences, Academy of mathematics and Systems Science; *Z. Wang,* HiSilicon Technologies Co., Ltd.; *N. Wang,* Hisilicon, Huawei; *W. Zhang,* HiSilicon Technologies Co., Ltd.; *Y. Huang,* Hisilicon, Huawei

A7.2 DIST: Deterministic In-System Test with X-masking
J. Tyszer, B. Wlodarczak, Poznan University of Technology; *G. Mrugalski, J. Rajski*,* Siemens Digital Industries Software

A7.3 Test Generation for an Iterative Design Flow with RTL Changes
J. Joe, I. Pomeranz,* Purdue University; *N. Mukherjee, J. Rajski,* Siemens Digital Industries Software

SESSION B7 Magic Kingdom Ballroom 2
Low-Power and Test
H.-P. Wen (Chair)

B7.1 Understand VDDmin Failures for Improved Testing of Timing Marginalities
A. Singh,* TU Delft

B7.2 Multiple Guard Bands for Low Power Consumption
W-C. Lin, C-H. Hsieh, J-M. Li, C. Chen,* National Taiwan University; *E-W. Fang,* MediaTek Inc.; *S-Y. Hsueh,* MediaTek inc.

B7.3 Comprehensive Power-Aware ATPG Methodology for Complex Low-power Designs
L. Manchukonda, E. Tsai, K. Abdel-Hafez,M. Dsouza, K. Natarajan,* Synopsys; *S. Lai, W. Hsueh,* MediaTek

.

Session Break

Thursday session refreshment break in the exhibit hall.
10:00 a.m.– 10:30 a.m.

SESSION C7 Magic Kingdom Ballroom 3

Special Session: Design-for-Verification (DfV): A New Direction in Design Qualification

Y. Zorian (Organizer)

A. Majumdar (Moderator)

Presenter: *D. Akselrod,* AMD

Panelists:

S. Millican, Auburn University

S. Sunter, Siemens

A. Sharma, Synopsys

S. Huhn, University of Bremen

SESSION D7 Magic Kingdom Ballroom 4

Panel 4: Automotive Safety & Security Interoperability

Organizer: Nir Maor, QualComm

Moderator: Yervant Zorian, Synopsys

Panelists:

- Sohrab Aftabjahani, Intel
- Luca Di Mauro, Arm
- Joytika Athavale, Nvidia
- Nir Maor, Qualcomm
- Jason M Fung, Intel
- P. V. Pillai, Texas Instruments
- Thiyagu Loganathan, Infineon

SESSION E7 Grand Ballroom South AB

Industrial Practices from ITC India

P. Wohl (Chair)

E7.1 TSV BIST Repair: Design-For-Test Challenges and Emerging Solution for 3D Stacked IC's

S. Akkapolu, Vaishnavi G, S. R. Malige, AMD

E7.2 Selective Multiple Capture Test (SMART) XLBIST

P. Wohl, J. Waicukauski, V. Kumar K S, A. Bhat, R. Karmakar, Synopsys*

E7.3 Transfer-Matrix Abstractions to Analyze the Effect of Manufacturing Variations in Silicon Photonic Circuits

P. Agnihotri, P. Kalla, S. Blair***,** The University of Utah

WORKSHOPS	Thursday, September 29 Friday, September 30	4:00 p.m. – 6:30 p.m. 8:30 a.m. – 4:00 p.m.

ART2022: IEEE Automotive Reliability, Test & Safety Workshop 2022
Magic Kingdom Ballroom 1

The ARTS workshop focuses exclusively on test, reliability and Safety of automotive and mission-critical electronics, including design, manufacturing, burn-in, system-level integration and in-field test, diagnosis and repair solutions, as well as architectures and methods for reliable and safe operations under different environmental conditions. With increasing system complexity, security, stringent runtime requirements for functional safety, and cost constraints of a mass market, the reliable operation of electronics in safety-critical domains is still a major challenge. This edition of the ARTS Workshop offers a forum to present and discuss these challenges and emerging solutions among researchers and practitioners alike.

Program Highlights:

- After the opening session of Thursday, Sundarrajan Subramanian , Qualcomm Vice President, will give the first Keynote speech on *"Journey from Mobile to Automobile: Leverage Learn Lead"* .
- Friday will start start with Vasanth Waran , Synopsys Senior Director, who will give the second Keynote speech on *"Evolution and Trends driving the Automotive Architecture and Ecosystems of the future"* .
- Four technical sessions will focus on:
    - *Advanced BIST design*
    - *NVM oriented reliability*
    - *In-field testing*
    - *Simulation and fault simulation techniques.*
- Technical sessions will be interleaved with a special session with a speech on "*The Accellera Functional Safety Standard: enabling automation, interoperability and traceability"* given by Alessandra Nardi , Accellera FS WG Chair.

.
General Chair: Yervant Zorian,
Program Chair: Paolo Bernardi
ART Web Page*:* *http://art.tttc-events.org/*

Second IEEE International Workshop on Silicon Lifecycle Management (SLM)
Magic Kingdom Ballroom 4

With increasing system complexity, security, stringent runtime requirements for functional safety, and cost constraints of a mass market, the reliable and secure operation of electronics in safety- critical, enterprise servers and cloud computing domains is still a major challenge. While traditionally design time and test time solutions were supposed to guarantee the in-field dependability and security of electronic systems, due to complex interaction of runtime effects from running workload and environment, there is a great need for a holistic approach for silicon lifecycle management, spanning from design time to in-field monitoring and adaptation. Therefore, the solutions for lifecycle management should include various sensors and monitors embedded in different levels of the design stack, access mechanisms and standards for such on-chip and in- system sensor network, as well as data analytics on the edge and in the cloud. The SLM Workshop offers a forum to present and discuss these challenges and emerging solutions among researchers and practitioners alike.

SLM include three keynote addresses and five technical sessions.
See the SLM Web Page for the complete SLM Program.

General Chair: Yervant Zorian, *zorian@synopsys.com*
Program Chair: Mehdi Tahoori
SLM Web Page: https://people.rennes.inria.fr/Marcello.Traiola/SLM22/index.html

Workshop Registration for Both Workshops

All workshop participation requires registration. Workshop registration includes the opening address, technical sessions, digest of papers, workshop reception, break refreshments, continental breakfast and lunch.
You may register onsite at regular rates at the ITC registration counter *Admission for onsite registrants is subject to availability.*

Workshop Reception

All registered workshop participants are invited to a reception to be held 7:00 p.m. – 9:00 p.m. on Thursday, September 29 at the Adventure Lawn.

Workshop Schedule

The workshops will all adhere to the same schedule:

Thursday, September 29

Registration	7:30 a.m. – 5:00 p.m.
Opening Address	4:00 p.m. – 5:00 p.m.
Technical Sessions	5:00 p.m. – 6:30 p.m.
Reception	7:00 p.m. – 9:00 p.m.

Friday, September 30

Technical Sessions	8:00 a.m. – 4:00 p.m.

Note: Workshop schedule is subject to change

FRINGE TECHNICAL MEETINGS **See registration desk for schedule.**

Castle C

ITC STEERING COMMITTEE

Teresa. McLaurin, ARM, *General Chair*
Jennifer Dworak, Southern Methodist University, *Past General Chair*

ARRANGEMENTS
Jill Sibert, Raspberry Communications, *Chair*

EXHIBITS
Chen-huan Chiang, Intel, *Chair*

FINANCE
Kenneth Mandl, *Chair*

MARKETING
Ron Press, Siemens, *Chair*
Scott Davidson, *Vice Chair*

PLANNING
Gordon Roberts, McGill University, *Chair*
William Lowd, BZ International, *Vice Chair*

PROGRAM
Kuen-Jong Lee, National Cheng Kung University, *Chair*
Jeff Rearick, AMD, *Vice Chair*

TTTC WORKSHOPS AND TUTORIALS LIAISON
Yervant Zorian, Synopsys

MEMBERS
Shawn Blanton, Carnegie Mellon University
Anne Gattiker, IBM
Marc Hutner
Peter Maxwell
Li-C Wang, University of California, Santa Barbara

IEEE PHILADELPHIA SECTION REPRESENTATIVE
Peter Silverberg

TTTC REPRESENTATIVE
Peilin Song, IBM

Table of Contents

ITC PROGRAM COMMITTEE

S, Adham, *TSMC*
S. A. Aftabjahani, *Intel*
E. Amyeen, *Intel*
L. Anghel, *INP-TIMA Laboratory*
D. Armstrong, *Advantest*
R. Arnold, *Infineon Technologies*
B. Becker, *University of Freiburg*
G. Bhargava, *Qualcomm*
S. Blanton, *CMU*
K. Butler, *Advantest*
J. Carulli, *GLOBALFOUNDRIES*
K. Chakrabarty, *Duke University*
K. Chakravadhanula, *Cadence Design Systems*
A. Chatterjee, *Georgia Institute of Technology*
H. Chen, *MidiaTek*
V. Chickermane, *Cadence Design Systems*
G. Colon-Bonet, *Intel*
W. Dobbelaere, *ON Semiconductor*
J. Dworak, *Southern Methodist University*
F. Farahmandi, *University of Florida*
F. Frederixk, *ARM*
M. Fujita, *University of Tokyo*
A. Gattiker, *IBM*
P. Girard, *LIRMM*
S. Goel, *TSMC*
S. Goh, *Qualcomm*
U. Guin, *Auburn University*
S. Gupta, *University of Southern California*
S. Gupta, NVIDIA
M. Hashimoto, *Kyoto University*
C. He, *NXP*
T.-Y. Hsieh, National Sun Yat-sen University
J-L. Huang, *National Taiwan University*
S-Y. Huang, *National Tsing-Hua University*
T-C. Huang, *National Changhua University*
M. Inoue, *Nara Inst. of Science and Tech.*
M. Ishida, *Advantest*
Y. Iskander, *Microsoft*
H. Jiao, *Peking University*
Y. Jin, *The University of Florida*
R. Kapur, Synopsys
N. Karimi, *University of Maryland*
R. Karri, *Polytechnic Institute of NYU*
H. Kobayashi, *Gunma University*
J. Lee, *National Taiwan University*
J-F Li, *National Central University*
X. Li, *Chinese Academy of Science*
Y. Li, *University of Chicago*
J-J. Liou, *National Tsing Hua University*
S.-K. Lu, *National Taiwan University*
Y. Makris, *University of Texas at Dallas*
EJ. Marinissen, *IMEC*
P. Maxwell
T. McLaurin, *ARM*
S. Natarajan, *Intel*
P. Nigh, *Broadcom*
P. Pant, *Inteal*
R. Parekhji, *Texas Instruments India*
K. Peng, *ARM*
M. Portolan, *TIMA*
J. Rajski, *Siemens*
S. Ravi, *Texas Instruments*
G. Roberts, *McGill University*
O. Sinanoglu, *New York University Abu Dhabi*
P. Song, *IBM*
F. Su, *Intel*
M. Tahoori, *Karlsruhe Institute of Technology*
S. Teehan, *IBM*
M. Tehranipoor, *University of Florida*
J. Tyszer, *Poznan University of Technology*
H. von Staudt, *Dialog Semiconductor*
H. Walker, *Texas A&M University*
Li-C. Wang, *U. of California, Santa Barbara*
S.-J. Wang, *National Chung Hsing University*
H.-P. Wen, *National Chiao Tung University*
X. Wen, *Kyushu Institute of Thechnology*
L. Winemberg, *Intel*
P. Wohl, *Synopsys*
C-W. Wu, *National Tsing-Hua University*
H-J. Wunderlich, *University of Stuttgart*
F. Zhang, *Southern Methodist University*
Y. Zorian, *Synopsys*

ITC AWARDS

Program Committee Awards

Outstanding Contribution Awards in recognition of service to the IEEE International Test Conference Program Committee

25 Years of Service	
Shawn Blanton	
15 Years of Service	
Jeff Rearick	
Li-C Wang	
10 Years of Service	
David Armstrong	**Yiorgos Makris**
John Caroli	**Ozgur Sinanoglu**
Masahiro Fujita	
5 Years of Service	
Robert Aitken	**Rubin Parekhji**
Abhijit Chatterjee	**Srivaths Ravi**
Vivek Chickermane	**Srikanth Venkataraman**
Jennifer Dworak	**Xiaoqing Wen**
Patrick Girard	**LeRoy Winemberg**
Rohit Kapur	**Peter Wohl**
Kuen-Jong Lee	**Yervant Zorian**
Sammy Makar	

Steering Committee Awards

Meritorious Service Award
For major contributions and leadership of IEEE International Test Conference while serving as General Chair for 2021
Jennifer Dworak

Outstanding Contribution Award
For major contributions and leadership to IEEE International Test Conference while serving as Program Chair for 2021
Teresa McLaurin

Outstanding Contribution Awards
Outstanding Contribution Awards in recognition of service to the IEEE International Test Conference Steering Committee

35 Years of Service
Amy Gold
25 Years of Service
Bill Lowd
Jill Sibert
20 Years of Service
Scott Davidson
Gordon Roberts
15 Years of Service
Ron Press
5 Years of Service
Jennifer Dworak
Li-C Wang

ADVANTEST®

Visit Booth# 223 to Learn about Latest Test Technologies

Advantest

3061 Zanker Road
San Jose, CA 95134
Phone: 408-456-3600
http://www.advantest.com/

Booth 223

A world-class technology company, Advantest is the leading producer of automatic test equipment (ATE) for the semiconductor industry and a premier manufacturer of measuring instruments used in the design and production of electronic instruments and systems. Its leading-edge systems and products are integrated into the most advanced semiconductor production lines in the world. The company also focuses on R&D for emerging markets that benefit from advancements in nanotech and terahertz technologies and has introduced multi-vision metrology scanning electron microscopes essential to photomask manufacturing, as well as groundbreaking 3D imaging and analysis tools. Founded in Tokyo in 1954, Advantest established its first subsidiary in 1982 in the USA and now has subsidiaries worldwide. More information is available at www.advantest.com.

Advanced Test Equipment Corp

10401 Roselle Street

San Diego, CA 92121

Phone: 800-404-ATEC (2832)

https://www.atecorp.com/

Booth 309

Caliber Interconnect Solutions

https://caliberinterconnect.com/servicedetails/IC_Test_Engineering

Booth 325

As a leading Semiconductor Test service provider, Caliber
Interconnects has been providing best-in-class full turnkey solutions to 150+ global customers for the past two decades.

Our 600+ engineers are steeped in technology innovation and have a unique combination of expertise to provide a maximum value proposition to our customers. We have been providing cost-effective solutions across products on multiple verticals including IC test engineering (ATE & Bench), IC packaging Design, Design, SI/PI simulation and manufacturing of high-speed / high-density PCBs (including ATE probe / final / system level test boards), and embedded system/power electronics solutions. Our test engineering services include new product introduction, test platform conversions, sustaining product maintenance such as test time optimization and yield improvement, multi-site solutions, characterization, and program releases.

Chroma ATE, Inc.

7 Chrysler

Irvine, CA 92618

Phone: 949-421-0355 x128

Fax: 949-421-0353

http://www.chromaus.com

Booth 315

Chroma ATE Inc. is a world-leading designer and manufacturer of complete turn-key , IC thermal management and automated IC Handling solutions. Specializing in integrated and fully automated turn-key electronic test and MES solutions for the semiconductor, front and back-end test spaces. Chroma is driven to provide unique, tailored solutions, and technical support to help our US-based customers excel in today's high demanding environment.

D|R|Yield

Opernring 4 8010

Graz Austria

Phone: **+43 316 225 7140**

https://dryield.com/

Booth 123

DR YIELD is the premier global provider of YieldWatchDog and the innovative leader in Big Data analytics.
Our software, YieldWatchDog is the smart solution for semiconductor data visualization and automated process control. More specifically, YieldWatchDog is the powerful yield management software for the integration, advanced analysis and enhanced visualization of all chip manufacturing and test data. It is capable of recognizing patterns and automatically notifies you if any irregularities occur. Using patented data aggregation technology and advanced algorithms, YieldWatchDog quickly integrates even large amounts of data into one large-scale, highly compressed database.
YieldWatchDog's user-friendly and intuitive interface gives you deep insight into your data.
YieldWatchDog is a customizable, fully scalable, turnkey solution that saves on engineering time and IT infrastructure costs. Visit our website for more information: https://dryield.com/

Ironwood Electronics

1335 Eagandale Court

Eagan, MN 55121

Phone: 952-229-8200

Fax: 952-229-8201

http://ironwoodelectronics.com

Booth 111

Includes 75 GHz bandwidth sockets for BGA and QFN, only slightly larger than IC with integral heatsink for medium power and optional heatsinking to over 100 watts. Up to 500k insertions. Adapters for prototype, package conversion, and more. Quick-Turn volume adapters are our specialty

Micro Control Company

7956 Main Street NE
Minneapolis, MN 55432
Phone: 1-800-328-9923
http://www.microcontrol.com

Booth 222

Micro Control Company is the test with burn-in expert. Devices that successfully complete a burn-in cycle in a Micro Control burn-in with test system stimulation are proving significantly more reliable for long-term use. Electronic stimulation is applied during the burn-in cycle Stressing the devices during burn-in causes devices that are going to fail, to fail early. By monitoring the devices as they are detected and eliminated from the lot.

Roos Instruments,Inc.

2285 Martin Avenue, C

Santa Clara, CA 95050

Phone: (408) 748-8589

http://www.roos.com

Booth 210

Roos Instruments is the premier supplier of highly automated test solutions for wireless devices. Our system's performance and technical expertise are the tools our customers rely on to meet the challenges of next generation products.

Fill in Your Exhibit Hall Passport for Prizes

All registered attendees will receive a passport in their conference bag. Get your passport stamped Tuesday and Wednesday while visiting exhibitor booths and at least one Corporate Forum session. Drop your completed passport into the collection box located in the exhibit hall, and be eligible for the drawing at 4:00 p.m. on Wednesday in the exhibit hall. You need not be present at the time of drawing to win.

Please see the full instructions included with your passport for details.

Table of Contents

EXHIBITORS

Siemens

8005 SW Boeckman Road

Wilsonville, OR 97070

https://eda.sw.siemens.com/en-US/ic/tessent/

Booth 115

Siemens is the technology and market leading provider of design-for-test solutions. With the industry's only comprehensive hierarchical DFT offering, our solutions enable our customers to achieve the lowest cost of test, highest test quality, fastest yield ramps and meet the most rigorous functional safety requirements demanded by the automotive market's ISO 26262 standard.

Synopsys

690 E Middlefield Road

Mountain View, CA 94043

Phone: 650-584-5000

Fax: 650-584-4249

http://www.synopsys.com

Booth 306

The Synopsys TestMAX™ family offers unparalleled test quality and efficiency, with tight integration across the Synopsys Fusion Design Platform to enable faster turnaround time while uniquely meeting both design and test goals concurrently.

TDK-Lambda

405 Essex Road

Neptune, NJ 07753

Phone: +1 732 922 9300

Fax: +1 732 922 1441

https://www.us.lambda.tdk.com/

Booth 227

TESEC

1225 W. 190th Street, Suite 325

Gardena, CA 90248

Phone: 1-480-829-6879

http://www.tesecinc.com/

Booth 323

Tesec is a world leader in power semiconductor test and automation. We provide high-volume production and engineering test solutions for a variety of applications including High-Power & High-Reliability devices, MEMS, and WLCSP/Strip-Test. The leading provider of yield improvement.

Test Spectrum

http://testspectrum.com/home/

Booth 226

Test Spectrum is a recognized leader in semiconductor test solutions. We provide software products that are essential tools for every test engineer and world class engineering services in test software and test hardware development. We are ITAR Certified.

Our customers include fabless semiconductor companies, integrated device manufacturers (IDMs), automated test equipment companies (ATE), test and assembly houses, and IP companies from all across the globe.

Founded in 1999 in Austin, Texas, Test Spectrum is an independent corporation with one goal in mind – to provide cutting edge technical solutions to the semiconductor test community. Our team is considered to have the best and brightest test development talent serving the semiconductor industry today.

TSE

http://www.tse21.com/

Booth 329

TSSI

920 SW Sixth Avenue

Portland, OR 97204

Phone: +1 503-764-2308

https://www.tessi.com/

Booth 317

Founded in 1979, TSSI is a worldwide leader in design-to-test conversion and validation software solutions. Our all-in-one graphical user interface allows all tools available at your fingertips, and data to be visualized throughout the vector translation process. Vector translation should not be a blind-conversion where extra steps are needed to even know whether the output patterns are correct. Also come to see how TSSI VirtualTester reduces silicon bring-up time from months to hours, and how 100% test patterns worked the first time. If visiting our physical booth in-person at Disneyland Hotel, come by to get a chance to win an Apple product!

Test Technology Technical Council

Phone: 540-937-8280

http://tab.computer.org/tttc

Booth 309

TTTC's goals are to contribute to our members' professional development and advancement, to help them solve engineering problems in electronic test, and to help advance the state-of-the art.

UNITES Systems

Phone: 503-555-1212

https://unites-systems.com//

Booth 324

UNITES Systems a.s. is on the market since 1991. Our main focus is on development and production of dedicated test and measurement systems, mainly ATE solutions for discrete semiconductors (such as MOSFETs, IGBTs, Diodes, BJTs and Power modules) with hundreds of installations worldwide. Recently with emphasis on SiC and GaN semiconductors. Apart from this, UNITES also develops and produce platforms for functional and in-circuit testing of assembled PCB testing (PCBA).

Table of Contents

Versatile Power

743 Camden Ave.

Campbell, CA 95008

Phone: 408-341-4604

Fax: 408-341-4601

https://versatilepower.com

Booth 322

Versatile Power has a long history of designing robust power supplies for military, industrial, commercial, laboratory and medical applications. Founded in 2002, Versatile Power offers a line of standard power supplies as well as custom-design power solutions. All of our products are designed and manufactured in the US.

Xallent Inc.

https://xallent.com/

Booth 326

yieldHUB

https://www.yieldhub.com/

Booth 307

With today's added pressures of time to market, along with the high cost of manufacturing, and material shortages, it's never been a better time for semiconductor companies and fabless startups to invest in a yield management platform. yieldHUB was designed to offer modern automated solutions for all yield management challenges.

Smart engineering is at the core of our platform, which was built so engineers can easily access and analyze data with unrivaled speed and accuracy. As volume grows, yieldHUB users can analyze and stack hundreds and even thousands of wafers at the same time using our cloud product on a web browser. Your engineers will be able to monitor production from any device no matter where they are.

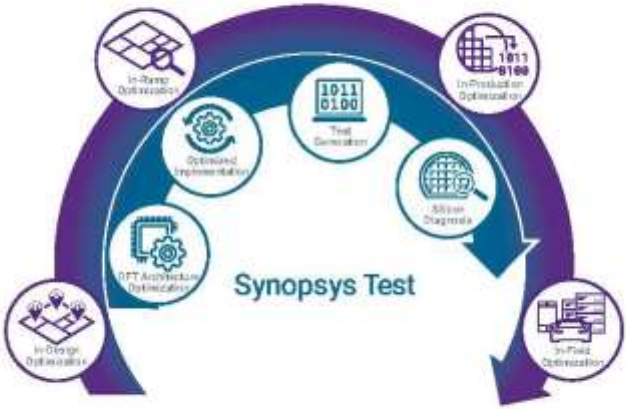
The yieldHUB platform offers exclusive and unique features to its customers, combined with intuitive design, innovative communication tools, and help from our team of highly experienced experts. We've helped improve the yield for manufacturers of 60 billion chips in the past year.

You could be just a few clicks away from having all your yield management problems solved by our team today.
Visit www.yieldhub.com to get started.

SYNOPSYS®

Synopsys Test and SLM Solutions

Synopsys SLM



Synopsys Test and Silicon Lifecycle Management (SLM) solutions encompass integrated tools, IP and methodologies to test, monitor and analyze SoCs, providing actionable insights at every phase of the device lifecycle.

To learn more visit:
www.synopsys.com/slm
www.synopsys.com/test

SYNOPSYS®
Silicon to Software™

EXHIBITOR BOOTH LOCATIONS

Table of Contents

Exhibits Floor Plan