2022

INTERNATIONAL TEST CONFERENCE

september 25-30, 2022

hybrid | disneyland/anaheim, ca

ITC Welcome Message

We are back live and what a grand place to have our first live event in three years; Disneyland! We have a fantastic program that addresses new test technology challenges that significantly affect today's electronic products!

ITC is the world's premier conference dedicated to electronics test. This year's ITC continues with its mission to play a unique role as an **information sharing forum,** where the wide range of its offerings allows ITC participants to learn, network and conduct business. This year's program includes a top-notch technical program, vibrant exhibitors, information-packed **tutorials**, interactive technical **panels**, two focused **workshops**, as well as the all-important networking that these events can provide. The technical program has been designed to optimize personal interactions on all levels. This year's program will include papers from a pool of impressive submissions and solicited papers. Of these submissions, a large number will focus on AI, automotive, memory, and hardware security. In complement to the paper presentations, there will be special sessions on hardware security certification, chiplet integration, silicon lifecycle management, computing in memory, as well as design and test of high-power compound devices and quantum electronics.

We are continuing and expanding on the inclusion of the Industrial Practice papers sessions as ITC has a very strong focus on industry practice as well as industry and academia advances. The three **keynotes** will encompass the past, present and future of our industry. In addition, there will be a **visionary talk** on AI accelerators.

ITC 2022 features a vibrant **exhibition** showcasing relevant companies. The exhibition will serve as a convenient one-stop-shop for all the elements of test technology.

In the past 53 years, ITC has helped globalize our industry and wants to continue to do so in the future. This year's return to a live event will enable us to embrace all of the features of the conference we have missed such as personal interaction and networking. Join us for the Wine and Cheese event after the Monday evening panel which kicks off ITC 2022. The ITC Grand Reception will be held Tuesday evening on the beautiful Adventure Lawn.

Last, but not least, I would like to recognize the enormous efforts of the multitude of dedicated volunteers who made ITC possible by donating their time, expertise, and enthusiasm. Without their hard work and dedication, ITC would not be possible. Please feel free to contact us if you would like to join our exciting team in the future.

ITC is the premier event for networking, where professionals from all over the world converge to sharpen skills, exchange ideas and do business. Join us, throughout the conference, for networking activities to unwind at the "Happiest Place on Earth", Disneyland!

Teresa McLaurin
General Chair

Kuen-Jong Lee
Program Chair

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	Sunday	Monday	Tuesday	Wednesday	Thursday	Friday
12 Half-Day TTTC Tutorials A great way to prepare for the ITC Technical program	●	●				
Four Panels		●	●	●	●	
Plenary Sessions, 3 Keynotes, 1 Visionary Talk			●	●	●	
Over 90 Technical Presentations			●	●	●	
World-Class Exhibits			●	●	●	
Corporate Forum The latest technical innovations from our exhibitors and corporate supporters			●	●		
35 Posters				●		
Two-Day Workshops Two to choose from					●	●

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SUNDAY, SEPTEMBER 25 – HALF-DAY TUTORIALS			
8:30 a.m. – 12:00 p.m.	Tutorial 1 Dependability and Testability of AI Hardware	Tutorial 2 Early System Reliability Analysis for Cross-layer Soft Errors	Tutorial 3 Device-Aware Test for Emerging Memories
1:00 p.m. – 4:30 p.m.	Tutorial 4 Computation in memory: Technologies, Design, Test and Reliability	Tutorial 5 Mixed-Signal DFT and BIST: Trends, Principles and Solutions	Tutorial 6 Scan Test Escapes, New Fault Models, and the Effectiveness of Functional System Level Tests

MONDAY, SEPTEMBER 26 – HALF-DAY TUTORIALS			
8:30 a.m. – 12:00 p.m.	Tutorial 7 Silicon Lifecycle Management for Emerging SOCs	Tutorial 8 Testing and Monitoring of Die-2-Die interconnects in 2.5D/3D IC	Tutorial 9 Domain-Specific Machine Learning in Semiconductor Test
1:00 p.m. – 4:30 p.m.	Tutorial 10 Automotive Safety, Reliability and Test Solutions	Tutorial 11 SoC Security Verification	Tutorial 12 Advances in Defect-Oriented Testing
4:30 p.m. – 6:00 p.m.	Panel 1- **An Industry-wide Dialog on Chiplets and Heterogeneous Integration**		

TUESDAY, SEPTEMBER 27 – TECHNICALSESSIONS					
9:00 a.m. – 10:30 a.m.	Plenary – Opening Session Keynote: Make Computing Count: Some Grand Opportunities for Testing, Parthasarathy Ranganathan, Google				
10:30 a.m. – 5:30 p.m.	Exhibits				
11:00 a.m. – 12:00 p.m.	Diamond Supporter Presentation				
12:00 p.m. – 2:00 p.m.	Lunch and Corporate Forum				
2:00 p.m. – 3:30 p.m.	Session A1 New Frontiers in Fault Modeling	Session B1 Innovation and Machine Learning I	Session C1 Diagnosis and Debug	Session D1 TTTC McCluskey PhD Competition	Session E1 Special Session Dedicated to the Memory of T. W. Williams, W. Maly and D. Pradhan
4:00 p.m. – 5:30p.m.	Panel 2 Are Last Century's Test Techniques Suitable for 21st century Silent Errors?	Session B2 Innovation with Machine Learning II	Session C2 New Frontiers in Test Content Optimization	Session D2 Test of HW Accelerators I	Session E2 Special Session: Experiences in Silicon Lifecycle Management
6:00 p.m. – 8:00 p.m.	ITC Welcome Reception				

WEDNESDAY, SEPTEMBER 28 – TECHNICAL SESSIONS					
9:00 a.m.–10:30 a.m.	Plenary Session Keynote: The Future of High Performance Computing Beyond Moore's Law, *John Shalf.* Lawrence Berkeley National Labs Visionary Talk: Ultra Low-Power AI Accelerators for AIoT, *Tim Cheng,* The Hong Kong University of Science and Technology				
9:30 a.m. – 4:30 p.m.	Exhibits				
10:30 a.m. – 11:00 a.m.	Coffee Break				
11:00 a.m.–12:30 p.m.	Session A3 Hardware Security I	Session B3 Latest on Wafer Map Analytics	Session C3 Memory Test/Diagnosis	Session D3 Special Session on Compute-In-Memory	Session E3 Industrial Practices I
12:30 p.m.–2:30 p.m.	Lunch Poster Presentations Corporate Forum – 1:30 p.m. – 2:30 p.m.				
2:30 p.m.–4:00p.m.	Session A4 Hardware Security II	Session B4 Test of HW Accelerators II	Session C4 Memory Test/Repair	Session D4 Automotive I	Session E4 Industrial Practices II
4:00 p.m.–4:30p.m.	Coffee Break				
4:30 p.m.–6:00 p.m.	Session A5 Special Session on HW Security Certification	Session B5 Analog Testing	Session C5 Panel 3: Performing RAS in Today's Mission Critical Systems	Session D5 Automotive: Special Session on High-Power Electronics	Session E5 Analog Test, Diagnosis, Test Cost, All-In-One

Registration Hours

Sunday, September 25: 7:30 a.m. – 3:00 p.m.

Monday, September 26: 7:30 a.m. – 5:00 p.m.

Tuesday, September 27: 8:00 a.m. – 6:00 p.m.

Wednesday, September 28: 8:00 a.m. – 4:00 p.m.

Thursday, September 29: 8:00 a.m. – 3:00 p.m.

Friday, September 30: 7:30 a.m. – 12:00 p.m.

Registration is closed from 12:00 p.m. to 1:00 p.m. Tuesday to Thursday,

and 11:00 a.m. to 1:00 p.m. Sunday and Monday

THURSDAY, SEPTEMBER 29 – TECHNICAL SESSIONS					
9:00 a.m. – 10:00 a.m.	Plenary Session Keynote: What Did We Learn in 120 Years of DFT and Test? *Grady Giles, Mike Bienek, & Tim Wood,* AMD				
9:30 a.m. – 1:00 p.m.	Exhibits				
10:00 a.m. – 10:30 a.m.	Coffee Break				
10:30 a.m.–12:00 p.m.	Session A6 Special Session on Test of Quantum Circuits	Session B6 Scan-Based Learning and Diagnosis	Session C6 Special Session: Road to Chiplets: UCIe	Session D6 Automotive II	Session E6 Industrial Practices III
12:00 p.m. – 1:30 p.m.	Lunch				
1:30 p.m.–3:00 p.m.	Session A7 Test Generation	Session B7 Low Power and Test	Session C7 Special Session: Design-for-Verification (DfV): A New Direction in Design Qualification	Session D7 Panel 4: Automotive Safety & Security Interoperability	Session E7 Special Session: Industrial Practices from ITC India

THURSDAY, SEPTEMBER 29 – WORKSHOPS		
4:00 p.m. – 5:00 p.m.	ART 2022: IEEE Automotive Reliability and Test & Safety Workshop 2022 Plenary1: Opening, Keynote	2nd IEEE Intl Workshop on Silicon Lifecycle Management (SLM) Plenary1: Opening, Keynote

FRIDAY, SEPTEMBER 30 – WORKSHOPS		
9:00 a.m. – 4:00 p.m.	ART 2022: IEEE Automotive Reliability and Test & Safety Workshop 2022	2nd IEEE Intl Workshop on Silicon Lifecycle Management (SLM)

All times are Pacific Daylight Savings Time

TTTC TEST TECHNOLOGY EDUCATION PROGRAM (TTEP) 2022

The Tutorials & Education Group of the IEEE Computer Society Test Technology Technical Council (TTTC) organizes a comprehensive set of Test Technology Tutorials to be held in conjunction with several TTTC-sponsored technical meetings worldwide. The mission of the Test Technology Educational Program (TTEP) is to serve test and design professionals by offering fundamental education and expert knowledge in state-of-the-art test technology topics. TTEP offers tutorial participants the opportunity to earn official certification from IEEE Computer Society TTTC. Each half-day tutorial corresponds to two TTEP units. Upon completion of 16 TTEP units, official recognition in the form of an IEEE TTTC Test Technology Certificate will be presented to the participant. For further information regarding TTEP, please visit http://ttep.tttc-events.org/ttep/index.html

At ITC 2022, TTTC/TTEP is pleased to present 12 **half-day tutorials** on topics of current interest to test professionals and researchers. All tutorials qualify for credit towards IEEE TTTC certification under the TTEP program. Six tutorials are held on Sunday, September 25. Six tutorials will be held on Monday, September 26.
The **one-day** tutorial registration fee is for two tutorials—a morning tutorial and afternoon tutorial, both on the same day, e.g., Tutorial 1 and Tutorial 4 on Sunday. You may register for up to four tutorials (two consecutive tutorials on Sunday and two consecutive tutorials on Monday).
The **all-access pass** tutorial registration provides in-and-out access to all twelve tutorials over both days.
(see registration page or http://www.itctestweek.org for further information).

Sunday 8:30 a.m. – 12:00 p.m. PDT

TUTORIAL 1
Dependability and Testability of AI Hardware

Presenters: F. Su, H. Stratigopoulos, Y. Makris

Toward continued performance improvement despite the slowed-down physical device scaling, adoption of bold and radical innovations in computer architectures has recently accelerated. One such trend focuses on computing architectures for AI hardware. While functionality of AI hardware still remains the main focus, testability and dependability of these new architectures need to be addressed before mainstream adoption. This tutorial covers the state-of-the-art in research and development of dependability and testability solutions for AI hardware (including digital or analog implementations of artificial neural networks (ANNs) and spiking neural networks (SNNs), used in accelerators and neuromorphic designs) and discusses challenges and future trends.

TUTORIAL 2
Early System Reliability Analysis for Cross-layer Soft Errors

Presenters: A. Bosio, S. Di Carlo, A. Salvino

In a world with computation at the epicenter of every activity, computing systems must be highly reliable even if miniaturization makes the underlying hardware unreliable. Techniques that guarantee high reliability are associated with high costs (reliability tax). Early reliability analysis can take informed design decisions to maximize reliability while minimizing the reliability tax. This tutorial focuses on early cross-layer reliability analysis considering the full computing continuum (from IoT/CPS to HPC applications), emphasizing soft errors. The tutorial will guide attendees from the definition of the problem down to the proper modeling and design exploration strategies considering the entire system stack.

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TUTORIAL 3
Device-Aware Test for Emerging Memories

Presenter: S. Hamdioui

This tutorial discusses conventional memory testing approach and applies it to two emerging memory technologies STT-MRAMs and RRAMs. Thereafter, it introduces Device-Aware Test (DAT) and demonstrates it based on two industrial memory designs: STT-MRAMs and RRAMs. DAT is a new test approach that goes beyond Cell-Aware Test; it does not assume that a defect in a device can be modeled electrically as a linear resistor (as the state-of-the art approach suggests), but it rather incorporates the impact of the physical defect into the technology parameters of the device and thereafter in its electrical parameters. Once the defective electrical model is defined, a systematic fault analysis is performed to derive appropriate fault models and subsequently test solutions. Industrial case studies for STTMRAM and RRAM show that DAT sensitizes realistic faults as well as new unique defects and faults that can never be caught with the traditional approach

Sunday 1:00 p.m. – 4:30 p.m. PDT

TUTORIAL 4
Computation in Memory: Technologies, Design, Test and Reliability

Presenter: M. Tahoori

Computation-in-Memory (CiM) paradigms are providing promising alternatives to tackle memory wall and power wall. CiM architectures based on emerging resistive non-volatile technologies are finding their way to efficiently implement deep learning cognitive tasks. Such technologies combine the storage and computation capabilities into the single device based on analog computing concepts. While many emerging technologies are being investigated for efficient implementation of such architectures and paradigms, there are several challenges related to test and reliability aspects of these technologies and architectures. From one side, these emerging devices are more prone to variations and defects, and from the other side, CiM paradigms crosses computation and storage boundaries, which were considered separated in traditional design-for-test (DfT) and design-for-reliability (DfR) solutions. This tutorial addresses design, test and reliability aspects of CiM technologies, circuits and architectures.

TUTORIAL 5
Mixed-Signal DFT and BIST: Trends, Principles and Solutions

Presenter S. Sunter

This tutorial explores systematic analog design-for-test and analog fault simulation, especially for automotive ICs. We review trends in ad hoc DfT, fault simulation, IEEE 1149.1/4/6/7/8/10 (briefly), 1687, and ISO 26262, then BIST for ADC/DAC, PLL, SerDes/DDR, and random analog. Essential principles of practical analog BIST are presented, then practical DfT techniques, from quicker analog defect simulation to over/under sampling methods that improve range, resolution, and reusability. We conclude with a discussion of the Analog Defect Coverage and Test Access standards (P1687.2, P2427), and measurement of ISO 26262 metrics.

TUTORIAL 6
Scan Test Escapes, New Fault Models, and the Effectiveness of Functional System Level Tests

Presenter: A. Singh

This tutorial aims at understanding the increasing use of functional system level tests (SLTs) as an additional final defect screen before processor SOCs are shipped for assembly. For this, we take an in-depth look at traditional scan based Stuck-at and TDF tests to understand potential sources of test escapes. We also extensively discuss the effectiveness of new test generation methodologies such as Cell Aware, Gate Exhaustive, Transistor Stuck-Open, and Timing Aware in plugging these structural test holes. Based on this, we identify failures that can still remain undetected by low cost scan structural tests, and require the use of expensive functional SLTs to achieve desired defect levels. In conclusion, we suggest strategies to minimize use SLTs without impacting defect levels.

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Monday 8:30 a.m. – 12:00 p.m. PDT

TUTORIAL 7
Silicon Lifecycle Management for Emerging SOCs

Presenters: Y. Zorian, F. Massoudi

Recent advances in automotive SOCs, artificial intelligence accelerators, and high-performance computing engines in data centers have led to an explosion in the adoption of emerging technology nodes and 3DIC/chiplet packages. This tutorial will present today's trends and discuss the resiliency challenges for such emerging SOCs. It will focus on optimizing the SOC health using advanced test, measurement and analytic solutions, such as on chip structural sensors, functional monitors, environmental sensors and embedded test & repair engines, typically utilized for managing the different silicon lifecycle stages: from silicon debug in early bring up stage to shorten the time-to-volume; to self-test and repair during volume production stage, in order to improve quality and yield; to power-on self-test in the field stage to address aging challenges; to periodic checking in-system to improve functional safety; and finally to fault tolerance and error correction during mission mode to address a range of transient errors. All of the above optimizations are materialized by on-chip and/or off-chip data analytics.

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TUTORIAL 8
Testing and Monitoring of Die-2-Die interconnects in 2.5D/3D IC

Presenter: S.-Y. Huang

With the evolution of multi-die integration into the era of interposer- or InFO-based 2.5-D ICs and/or TSV-based 3D stacked ICs, die-to-die interconnects could operate in a very high speed, with an end-to-end delay of only a few hundreds of picoseconds. Parametric defects (like small delay faults, resistive open/bridging faults, leakage faults, etc.) have been identified as potential threats to the yield and reliability of a 2.5D/3D IC product. Fortunately, various test and online monitoring methods have been developed to deal with this challenge and to guarantee the overall quality of the die-to-die interconnects in a 2.5D/3D IC product.

TUTORIAL 9
Domain-Specific Machine Learning in Semiconductor Test

Presenter: L-C. Wang

Applying Machine Learning (ML) in analytics of data from semiconductor test and manufacturing has received growing interests in years. This tutorial will approach ML from a domain specific perspective. We will introduce Domain-Specific Machine Learning (DSML) in semiconductor test and explain the fundamental difference between DSML and ML. In essence, DSML is applied in an iterative engineering process where the underlying data generator such as the production process, the test content, or the design, is being improved. In this iterative process, ML is applied to facilitate an engineer to move from one iteration to the next. In view of DSML, we will discuss common test data analytics practices including outlier analysis, wafer map pattern recognition, yield optimization, and cross-insertion predictive analysis, and explains their challenges and potential solutions. We will review the latest ML technologies in Foundation Models and discuss how they might find uses in DSML in semiconductor test.

Monday 1:00 p.m. – 4:30 p.m. PDT

TUTORIAL 10
Automotive Safety, Reliability and Test Solutions

Presenters: R. Mariani, Y. Zorian

With the fast-growing adoption of advanced technology nodes for automotive chips, this tutorial will discuss the implications of automotive quality, functional safety, and reliability on all aspects of automotive SOC lifecycle, while accelerating time to market for these semiconductor ICs. The automotive SOC lifecycle stages will include design, silicon bring-up, volume production, and particularly in-system operation. Today's automotive safety critical chips need multiple in-system modes, such as power-on and power-off self-test and repair (key-on/key-off), periodic in-field self-test during mission mode, advanced error correction solutions, etc. This tutorial will analyze these specific in-system test modes and the discuss the benefits of using ISO 26262 including its second edition, and several newer standardization efforts, to ensure that standardized functional safety requirements are met.

TUTORIAL 11
SoC Security Verification

Presenters: M. Tehranipoor, F. Farahmandi

The growing complexity of system-on-chips (SoCs) and the increased security requirements have made security verification a major challenge. It is imperative to develop security verification solutions as well as automatic CAD tools to identify and detect such vulnerabilities at pre-silicon while it is possible to change the design and address security vulnerabilities. The goal of this tutorial is to present (i) vulnerabilities introduced during various stages of the design life cycle, (ii) CAD tools and methodologies for security assessment, (iii) Countermeasure tools and methodologies for addressing each vulnerability, and (iv) challenges and research roadmap ahead.

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TUTORIAL 12
Advances in Defect-Oriented Testing

Presenters A. Singh, A. Glowatz

Recent experience indicates that traditional logic level stuck-at and TDF scan test methodologies can miss significant defectivity that is better captured by new defect-oriented fault models that explicitly target potential defect locations based on the layout. In this tutorial, we present the latest in defect-oriented test methodology, from its initial focus on cell internal defects, to the most recent advances that comprehensively cover inter-cell defects, as well as bridges and opens in the interconnect network. Timing aware cell aware tests also minimize timing slack for small delay defect detection. Test effectiveness is discussed based on volume data from a number of industrial studies.

Click on an Exhibitor Name to go to their Website

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** As of publication date*

The Corporate Forum track provides an opportunity for ITC exhibitors and supporters to present information on their latest products and services.

The **Corporate Forum** will be held on Tuesday, September 27 and Wednesday, September 28. All times are **Pacific Daylight Time**. Expect more titles and presenters.

Day	Time	Company	Title of Presentation
Tuesday	11:00 am-12:00 p.m.	Siemens	1. DFT to In-Life monitoring for dependable electronic systems. A. Gupta, Siemens 2. Reducing Design Effort, Test Time And Power With SSN in AWS Custom Silicon, D. Trock, Amazon 3. Advancements in DFT automation for 2.5D / 3D IC era, V. Neerkundar, Siemens 4. Structural Deterministic Test in Silicon Lifecycle, J. Rajski, Siemens
	12:00 p.m. – 12:30 p.m.	Synopsys	Test and Analytics: Enabling Silicon Lifecycle Management, R. Ruiz, Synopsys
	12:30 p.m. – 1:00 p.m.	Advantest	Enabling Leading-Edge Technologies in an Exascale Era, K. Schaub, Advantest
	1:30 p.m. – 1:45 p.m..	Chroma	Facing the Challenges in Automated Handling of Advanced IC Packaging, J. Hauck, Chroma
	1:45 p.m. – 2:00 p.m.	Galaxy	Galaxy Semiconductor Solutions, D. King, Galaxy
Wednesday	10:30 a.m – 10:40 a.m.	UNITES Systems	Testing SiC and GaN discrete semiconductors, O. Betak, UNITES Systems
	10:40 a.m. – 10:50 a.m.	Xallent Inc.	Thin Films Testing Up to 300X Faster, Kwame Amponsah, Xallent
	10:50 a.m. – 11:00 a.m.	yieldHUB	Revolutionize your yield management, C. S. Moore, yieldHub
	1:30 p.m. – 1:45 p.m.	Chroma	High Multisite Testing for Hi Fidelity True Wireless Stereo (TWS) Devices, E. Lin, Chroma
	1:45 p.m. – 2:00 p.m.	DR Yield	YieldWatchDog Solution for AI Test Data Analytics, K. Tropper, DR Yield
	2:00 p.m. – 2:15 p.m.	Caliber Interconnect Solutions	Value Proposition - Caliber Interconnect Solutions, M. Berry, Caliber
	2:15 p.m. – 3:00 p.m.	Roos Instruments, Inc.	Roos Cassini: Continuous Coverage to 110GHz, M. Roos, Roos

Tuesday 9:00 a.m. – 10:30 a.m.

Opening Remarks
Teresa McLaurin, *ITC 2022 General Chair*

ITC 2022 Program Introduction
Kuen-Jong Lee, *ITC 2022 Program Chair*

ITC 2021 Paper Awards Presentation
Teresa McLaurin, *ITC 2021 Program Chair*

TTTC Awards Presentation
Yervant Zorian

Keynote Address

Make Computing Count: Some Grand Opportunities for Testing

Parthasarathy Ranganathan
VP/technical Fellow, Google

Abstract: Moore's law is slowing down, stressing traditional assumptions around cheaper and faster systems every year. At the same time, growing volumes of data, smarter edge devices, and new, diverse workloads are causing demand for computing to grow at phenomenal rates. In this talk, we will discuss the trends shaping the future computing landscape, with a specific focus on the role of testing -- for correctness, agility, and performance -- and some grand challenges, and opportunities, for the field.
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About the speaker:
Partha Ranganathan is currently a VP, technical Fellow at Google where he is the area technical lead for hardware and datacenters, designing systems at scale. Prior to this, he was a HP Fellow and Chief Technologist at Hewlett Packard Labs where he led their research on systems and data centers.

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9:00 a.m. – 9:45 a.m.

Plenary 2: *J. Rearick* **(Chair)**

The Future of High Performance Computing Beyond Moore's Law

John Shalf *Lawrence Berkeley National Labs*

Abstract: The next decade promises to be one of the most exciting yet in the further evolution of computing. There are a number of developments that will change how we will compute in 10 years: the foreseeable end of Moore's law will lead to the exploration of new architectures and the introduction of new technologies in HPC; the rapid progress in machine learning in the last decade has led to a refocus of HPC towards large scale data analysis and machine learning; the feasibility of quantum computing has led to the introduction of new paradigms for scientific computing; meanwhile 30 billion IOT devices will push advances in energy efficient computing and bring an avalanche of data. I would like to compare the situation to a Cambrian explosion: the change in computing environment has helped creating a wide and complex variety of "organisms" that will compete for survival in the next decade. The HPC community will have to deal with this complexity and extreme heterogeneity, and decide what ideas and technologies will be the survivors. In this talk, I will talk about emerging strategies such as heterogeneous integration (advanced packaging) that are playing out across the industry to continue to extract performance from systems and make predictions of where things are going for 2025-2030.
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About the speaker: John Shalf is Department Head for Computer Science at Lawrence Berkeley National Laboratory, and recently was deputy director of Hardware Technology for the DOE Exascale Computing Project.
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9:00 a.m. – 10:00 a.m.

Plenary 3: *Y. Zorian* (Chair)

What Did We Learn in 120 years of DFT and Test?

Grady Giles, Mike Bienek, & Tim Wood *AMD*

Abstract: This interview-style discussion will feature three industry veterans whose careers have followed (and propelled) the growth in our field. We plan to reflect on how our industry has evolved, how this conference has reflected and driven that evolution, what lessons were learned, and what we can expect (and make happen) next. Along the way, we'll share some anecdotes, tell some stories, brag about some accomplishments, and humbly give some advice on things we found out the hard way (so that you don't have to).

About the speakers: Grady Giles, Mike Bienek, and Tim Wood are all members of the DFX team at AMD, with a combined 120+ years of experience in the industry.

Wednesday, September 28
9:45 a.m. – 10:30 a.m.

Visionary Talk 1: *K-J Lee* (Chair)

Ultra Low-Power AI Accelerators for AIoT – Compute-in-memory, Co-Design, and Heterogeneous Integration

Tim Cheng, *The Hong Kong University of Science and Technology*

Abstraxtr We will give an overview of the objectives and some recent progress in designing ultra-low-power AI accelerators for supporting a wide range of AIoT devices with powerful embedded intelligence. Specifically, we will discuss the roles of emerging memory and compute-in-memory for data-centric computing, application-specific co-design framework supporting light-weight deep learning which integrates neural network (NN) search, hardware-friendly NN compression and NN-aware architecture design for iterative co-optimization, as well as the critical role of 3D integration of processors and memory arrays for power, performance and size.

About the Speaker: Tim Cheng is currently Vice-President for Research and Development at Hong Kong University of Science and Technology (HKUST) and Chair Professor jointly in the Departments of ECE and CSE., music analysis/retrieval, image classification, medical/healthcare data analytics, and FinTech.

2:00 p.m. – 3:30 p.m. PDT

SESSION A1
New Frontiers in Fault Modeling
S. Adham (Chair)

A1.1 PEPR: Pseudo-Exhaustive Physical Region Testing
W. Li, D. Duvalsaint, R. Blanton, Carnegie Mellon University; *C. Nigh,* Qualcomm Technologies, Inc.; *S. Mitra,* Stanford University

A1.2 Error Model- A New Way of Doing Fault Simulation
N. Saxena, A. Lotfi, NVIDIA

A1.3 Using Custom Fault Modelling to Improve Understanding of Silicon Failures
S. Kundu, The University of Texas at Dallas; *G. Bhargava, L. Endrinal, L. Ranganathan,* Qualcomm Technologies Inc

SESSION B1
Innovation with Machine Learning I
K. Butler (Chair)

B1.1 DeepTPI: Test Point Insertion with Deep Reinforcement Learning
Z. Shi, M. Li, S. Khan, Q. Xu, The Chinese University of Hong Kong; *L. Wang,* Huawei Technologies Co., Ltd.; *N. Wang,* Hisilicon, Huawei; *Y. Huang,* Hisilicon, Huawei

B1.2 Efficient and Robust Resistive Open Defect Detection Based on Unsupervised Deep Learning
Y. Liao, Z. Najafi-Haghi, H-J. Wunderlich, B. Yang, University of Stuttgart

B1.3 RCANet: Root Cause Analysis via Latent Variable Interaction Modeling for Yield Improvement
X. Zhang, E. Young, The Chinese University of Hong Kong; *S. Hu, Z. Chen, S. Zhu, J. Hao,* Huawei Noah's Ark Lab; *P. Li, C. Chen,* HiSilicon; *Y. Huang,* Hisilicon, Huawei

SESSION C1
Diagnosis and Debug
S-Y Huang (Chair)

C1.1 Scaling Physically Aware Logic Diagnosis to Complex High Volume 7nm Server Processors
B. Nandakumar, S. Chillarige, M. Maheshwari, Cadence Design Systems; *R. Redburn, J. Zimmerman, N. L'Esperance, E. Dziarcak,* IBM

C1.2 Diagnosing Double Faulty Chains through Failing Bit Separation
C-S. Kuo, J-M. Li, B-H. Hsieh, National Taiwan University; *C. Nigh, M. Chern, G. Bhargava,* Qualcomm Technologies Inc

C1.3 Transient Fault Pruning for Effective Candidate Reduction in Functional Debugging
D-A. Yang, National Tsing Hua University, Department of Electrical Engineering; *J-J. Liou,* National Tsing Hua University, Department of Electrical Engineering; *H. Chen,* MediaTek Inc., Computing and AI Technology Group

SESSION D1
TTTC PhD Thesis Competition - Final Round
M. Portolan (Chair)

D1.1 Next Generation Design For Testability, Debug and Reliability Using Formal Techniques
S. Huhn, University of Bremen; *R. Drechsler,* University of Bremen, Germany

D1.2 Testing of Analog Circuits using Statistical and Machine Learning Techniques
S. Srimani, H. Rahaman, Indian Institute of Engineering Science and Technology

D1.3 AI-Driven Assurance of Hardware IP against Reverse Engineering Attacks
P. Charaborty S. Bhunia, University of Florida

SESSION E1
Special Session Dedicated To The Memory Of Tom W. Williams, Wojciech Maly and Dhiraj Pradhan
Y. Zorian (Chair)

E1.1 Wojciech Maly Memorial
A. Meixner, IBM*; P. Nigh,* Broadcom

***E1.2* Tom W Williams Memorial**
R. Mercer; S. Mitra, Stanford

***E1.3* Dhiraj K Pradhan Memorial**
A. Singh, Auburn U; *S. Gupta*, USC

4:00 p.m. – 5:30 p.m.

SESSION A2
Panel 2: Are Last Century's Test Techniques Suitable for 21st Century Silent Errors?
S. Chakravarty, S. Mitra (Organizers)
J. Rearick (Moderator)

SESSION B2
Innovation with Machine Learning II
H.-P. Wen (Chair)

B2.1 Neural Fault Analysis for SAT-based ATPG
J. Huang, Noah's Ark Lab, Huawei; *H-L. Zhen,* Noah's Ark Lab, Huawei; *N. Wang,* Hisilicon, Huawei; *H. Mao,* Noah's Ark Lab, Huawei; *M. Yuan,* Noah's Ark Lab, Huawei; *Y. Huang,* Hisilicon, Huawei

B2.2 Improving Test Quality of Memory Chips by a Decision Tree-Based Screening Method
Y-C. Cheng, M-D. Shieh, NCKU; *P-Y. Tan, C-W. Wu,* NTHU; *C-H. Chien-Hui Chuang, G. Liao,* TSMC

B2.3 Fault Resilience Techniques for Flash Memory of DNN Accelerators
S-K. Lu, Y-S. Wu, National Taiwan University of Science and Technology; *J-H. Hong,* National University of Kaohsiung; *K. Miyase,* Kyushu Institute of Technology

SESSION C2
New Frontiers in Test Content Optimization
M. Tahoori (Chair)

C2.1 Automatic Structural Test Generation for Analog Circuits using Neural Twins
J. Talukdar, A. Chaudhuri, K. Chakrabarty, Duke University; *M. Bhattacharya,* Synopsys

C2.2 DEFCON: Defect Acceleration through Content Optimization
S. Natarajan, A. Sathaye, C. Oak, N. Chaplot, S. Banerjee, Intel Corporation

C2.3 Low Capture Power At-Speed Test with Local Hot Spot Analysis to Reduce Over-Test
A. Srivastava, J. Abraham, Qualcomm Inc

SESSION D2
Test of HW Accelerators I
*K. Chakravadhanula (*Chair*)*

D2.1 A Multi-level Approach to Evaluate the Impact of GPU Permanent Faults on CNN's Reliability
J. Rodriguez Condia, J. Guerrero Balaguera, M. Sonza Reorda, Politecnico di Torino; *F. Fernandes dos Santos,* Institut National de Recherche en Sciences et Technologies du Numérique (INRIA); *P. Rech,* University of Trento

D2.2 Accelerating RRAM Testing with Low-cost Computation-in-Memory based DFT
A. Singh, M. Fieback, R. Bishnoi, F. Bradari, A. Gebregiorgis, S. Hamdioui, TU Delft; *R. Joshi,* IBM

D2.3 Compact Functional Test Generation for Memristive Deep Learning Implementations Using Approximate Gradient Ranking
S. Ahmed, Karlsruhe Institute Of Technology; *M. Tahoori,* Karlsruhe Institute of Technology (KIT), Faculty of Informatik

SESSION E2
Special Session: Experiences in Silicon Lifecycle Management
Y. Zorian, Synopsys (Organizer)
Swapnil Bahl, Meta (Chair)

E2.1 In-Field System Debug and Silicon Life Cycle Management of Compute Systems
S. Menon, R. Kuehnis, R. Kandula, Intel

E2.2 Sensor Aware Production Testing
F. Massoudi, A. Patel, K. Darbinian, Y. Zorian, Synopsys

E2.3 Empowering Secure and Reliable BIST Solution for Automotive SOCs
M. S. Julapati, *N. Shenoy*, Qualcomm; *G. Tshagharyan, K. Kyuregyan, G. Harutyunyan*, Synopsys

11:00 a.m. – 12:30 p.m. Pacific Daylight Time

SESSION A3
Hardware Security I
J. Dworak (Chair)

A3.1 RTL-FSMx: Fast and Accurate Finite State Machine Extraction at the RTL for Security Applications
R. Kibria, M. Rahman, F. Farahmandi, M. Tehranipoor, University of Florida

A3.2 TAMED: Transitional Approaches for LFI Resilient State Machine Encoding
M. Choudhury, M. Gao, S. Tajik, D. Forte, University of Florida

A3.3 Reliability Study of 14 nm Scan Chains and Its Application to Hardware Security
F. Stellari, P. Song, IBM

SESSION B3
Latest on Wafer Map Analytics
J. Li (Chair)

B3.1 Language Driven Analytics for Failure Pattern Feedforward and Feedback
M. Yang, Y. Zeng, University of California Santa Barbara; *L-C. Wang,* UCSB

B3.2 Wafer Map Defect Classification Based on the Fusion of Pattern and Pixel Information
Y. Liao, P. Genssler, H. Amrouch, B. Yang, University of Stuttgart; *R. Latty,* Advantest Europe GmbH

B3.3 WXAI: Wafer Defect Pattern Classification with Explainable Rule Based Decision Tree Methodology
K-C. Cheng, A-A. Huang, C-S. Lee, L-Y. Chen, P-Y. Liao, N-Y. Tsai, NXP Semiconductors Taiwan Ltd.; *K-M. Li,* National Sun Yat-Sen University; *S-J. Wang,* National Chung Hsing University

B3.4 Yield-Enhanced Probing Cleaning with AI-Driven Image and Signal Integrity Pattern Recognition for Wafer Test
N. Sinhabahu, J. Wang, NXP Semiconductors Taiwan Ltd.; *K-M. Li,* National Sun Yat-Sen University; *J-D. Li, S-J. Wang,* National Chung Hsing University

S ESSION C3
Memory Test/Diagnosis
S-K Lu (Chair)

C3.1 Fault Diagnosis for Resistive Random-Access Memory and Monolithic Inter-tier Vias in Monolithic 3D Integration
S-C. Hung, A. Chaudhuri, K. Chakrabarty, Duke University; *S. Banerjee,* Intel Corporation

C3.2 Fault Modeling and Testing of Memristor-Based Spiking Neural Networks
K-W. Hou, H-H. Cheng, C. Tung, National Tsing Hua University; *C-W. Wu,* NTHU; *J-M. Lu,* Industrial Technology Research Institute

C3.3 Fault-coverage Maximizing March Tests for Memory Testing
R. Feng, Y. Lin, Y. Lou, L. Gao, V. Gera, B. Li, V. Chowdary Nekkanti, A. Rajendra Pharande, K. Sheth, M. Thommondru, G. Ye, University of Southern California; *S. Gupta,* Purdue University

C3.4 Enhanced Data Pattern to Detect Defects in Flash Memory Address Decoder
J. Soh, C. He, NXP Semiconductors

SESSION D3
Special Session on In-Memory Computing Design and Test Challenges
S. Adham, S. Hamdioui, ***(Organizers)***
S*. Adham* (Chair)

D3.1 In-Memory Computing: History, Overview, Current and Future Directions
N. Shanhbag, Univ. of Illinois

D3.2 Testing Computation-in-Memory Architectures Based on Memristive Devices
S. Hamdioui, Delft, University

D3.3 Fully Digital Compute In Memory Design and Test Challenges
S. Adham, TSMC

SESSION E3
Industrial Practices I
P. Nigh **(Chair)**

E3.1 Application of Sampling in Industrial Analog Defect Simulation
M. Bhattacharya, B. Solignac, M. Durr, Synopsys

E3.2 Challenges for High Volume Testing of Embedded IO Interfaces in Disaggregated Microprocessor Products
E. Garita-Rodriguez, R. Rimolo-Donadio, R. Zamora-Salazar, Intel

E3.3 New R&R Methodology in Semiconductor Manufacturing Electrical Testing
A. Pagani, F. Brembilla, STMicroelectronics

2:30 p.m. – 4:00 p.m.

SESSION A4
Hardware Security II
P. Song (Chair)

A4.1 Modeling Challenge Covariances and Design Dependency for Efficient Attacks on Strong PUFs
H. Wang, W. Liu, H. Jin, Y. Chen, W. Cai, Huazhong University of Science and Technology

A4.2 ADWIL: A Zero-Overhead Analog Device Watermarking Using Inherent IP Features
U. Das, M. Muttaki, M. Tehranipoor, F. Farahmandi, University of Florida

A4.3 Circuit-to-Circuit Attacks in SoCs via Trojan-Infected IEEE 1687 Test Infrastructure
M. Portolan, Univ Grenoble Alpes, CNRS; *A. Pavlidis, H. Stratigopoulos,* Sorbonne Université LIP6; *G. Di Natale,* CNRS; *E. Faehn,* ST Microelectronics

A4.4 Hardware Root of Trust for SSN-based DFT Ecosystems
J. Tyszer, B. Wlodarczak, Poznan University of Technology; *J. Rajski, M. Trawka,* Siemens Digital Industries Software

SESSION B4
Test of HW Accelerators II
S. Gupta (Chair)

B4.1 Functional In-Field Self-Test for Deep Learning Accelerators in Automotive Applications
T. Uezono, Hitachi; *Y. He, Y. Li,* University of Chicago

B4.2 Defect-Directed Stress Testing Based on Inline Inspection Results
C. He, P. Grosch, O. Anilturk, J. Witowski, C. Ford, R. Kalyan, NXP Semiconductors; *J. Robinson, D. Price, J. Rathert, B. Saville,* KLA Corporation

B4.3 The Impact of On-chip Training to Adversarial Attacks in Memristive Crossbar Arrays
B. Paudel, S. Tragoudas, Southern Illinois University Carbondale

B4.4 RIBoNN: Designing Robust In-Memory Binary Neural Network Accelerators
S. Kundu, K. Basu, The University of Texas at Dallas; *A. Malhotra, S. Gupta,* Purdue University; *A. Raha,* Intel Corporation

SESSION C4
Memory Test/Repair
J. Yun (Chair)

C4.1 Configurable BISR Chain For Fast Repair Data Loading
W. Zou, B. Nadeau-Dostie, Siemens EDA

C4.2 Efficient Built-In Self-Repair Techniques with Fine-Grained Redundancy Mechanisms for NAND Flash Memories
S-K. Lu, S-C. Tseng, National Taiwan University of Science and Technology; *K. Miyase,* Kyushu Institute of Technology

C4.3 Analyzing the Electromigration Challenges of Computation in Resistive Memories
M. Mayahinia, Karlsruhe institute of technology (KIT); *M. Tahoori,* Karlsruhe Institute of Technology (KIT), Faculty of Informatik; *M. Perumkunnil, K. Croes, F. Catthoor,* IMEC

C4.4 DFT-Enhanced Test Scheme for Spin-Transfer-Torque (STT) MRAMs
Z-W. Pan, J-F. Li, National Central University

SESSION D4
Automotive I
P. Wohl (Chair)

D4.1 An innovative Strategy to Quickly Grade Functional Test Programs
P. Bernardi, A. Francesco, S. Quer, L. Cardone, A. Calabrese, D. Piumatti, A. Niccoletti, Politecnico di Torino; *D. Appello, V. Tancorre, R. Ugioli*, STMicroelectronics

D4.2 A Practical Online Error Detection Method for Functional Safety Using Three-Site Implications
K. Ioki, ROHM Co., Ltd.; *Y. Kai, K. Miyase, S. Kajihara*, Kyushu Institute of Technology

D4.3 PPA Optimization of Testpoints in Automotive Designs
B. Foutz, S. Singhal, P. Rai, K. Chakravadhanula, V. Chickermane, B. Nandakumar, S. Chillarige, C. Papameletis, S. Ravichandran, Cadence Design Systems

SESSION E4
Industrial Practices II
C-W Wu (Chair)

E4.1 Accurate Failure Rate Prediction Based on Gaussian Process Using WAT Data
M. Eiki, M. Kajiyama, T. Nakamura, Sony Semiconductor Manufacturing; *M. Shintani*, Kyoto Institute of Technology; *M. Inoue*, Nara Institute of Science and Technology

E4.2 4.5Gsps MIPI D-PHY Receiver Circuit for Automatic Test Equipment
S. Lee, C. Park, M. Kang, J. Won, H. Ryu, J. Choi, B. Yim, Samsung Electronics

E4.3 Optimization of Tests for Managing Silicon Defects in Data Centers
D. Lerner, B. Inkley, S. Sahasrabudhe, E. Hansen, A. Van De Ven, Intel Corporation

E4.4 Improving Structural Coverage of Functional Tests with Checkpoint Signature Computation
B. Niewenhuis, D. Varadarajan, Texas Instruments

E4.5 Zero Trust Approach to IC Manufacturing and Testing
B. Buras, Advantest; *C. Xanthopoulos, J. Kim, K. Butler*, Advantest America Inc

E4.6 Virtual Prototyping: Closing the Digital Gap between Product Requirements and Post-Si Verification & Validation
T. Nirmaier, M. Harrant, M. Huppmann, G. Pelz, Infineon Technologies

4:30 p.m. – 6:00 p.m.

SESSION A5
Special Session on HW Security Certification
T-Y Chan (Chair)

A5.1 Latest Cybersecurity Regulations, Certifications and Labeling Trends
R. Menda-Shabat, Winbond

A5.2 GlobalPlatform: 20 years of Security Evaluation on Secure Components
G. Bernabeu, GlobalPlatform

A5.3 Hardware Security in IoT Platforms and Certification
T.-Y. Chan, Winbond

SESSION B5
Analog Testing
H. M. von Staudt (Chair)

B5.1 ML-Assisted Bug Emulation Experiments for Post-Silicon Multi-Debug of AMS Circuits
***J-Y. Lei, A. Chatterjee*, Georgia Institute of Technology**

B5.2 A Path Selection Flow for Functional Path Ring Oscillators using Physical Design Data
***T. Kilian*, Infineon Technologies AG / Technical University of Munich; *M. Hanel, U. Schlichtmann*, Technical University of Munich; *D. Tille*, Infineon Technologies AG; *M. Huch*, Infineon Technology AG**

B5.3 IEEE P1687.1: Extending the Network Boundaries for Test
***M. Laisne, H. von Staudt*, Dialog Semiconductor - a Renesas Company; *A. Crouch*, Amida Technology Solutions, Inc.; *M. Portolan*, Univ Grenoble Alpes, CNRS; *M. Keim*, Siemens Digital Industries Software; *B. Van Treuren*, VT Enterprises Consulting Services; *J. Rearick*, Advanced Micro Devices; *S. Zuo*, Tailored Management**

SESSION C5
Panel 3: Performing RAS in Today's Mission Critical Systems
Y. Zorian (Organizer)
P. Benardi (Moderator)

SESSION D5
Automotive: Special Session on High-Power Electronics
***S-Y Huang*, National Tsing Hua University** (Organizer, Chair)

D5.1 The Importance and Demand Market of SiC Substrate Defect Testing,
W-C Chang, Industrial Technology Research Institute

D5.2 Validation of SPICE Models for Commercial SiC MOSFETs
H-Y Teng, Industrial Technology Research Institute

D5.3 Practical Design Experiences on a Multi-Voltage-Level Motor Driver System using a Power Inverter
C-C Chiu, Industrial Technology Research Institute

SESSION E5
Analog Test, Diagnosis, Test Cost, All-In-One
A. Singh (Chair)

E5.1 Efficient Low Cost Alternative Testing of Analog Crossbar Arrays for Deep Neural Networks
***K. Ma, A. Saha, C. Amarnath,A. Chatterjee*, Georgia Institute of Technology**

E5.2 Low Cost High Accuracy Stimulus Generator for On-chip Spectral Testing
***K. Bhatheja, S. Chaganti, D. Chen*, Iowa State University*; X. Jin, C. Dao, J. Ren, A. Kumar, D. Correa, M. Lehrmann, T. Rodriguez, E. Kingham, J. Knight. A. Dobbin, S. Herrin, D. Garrity*, NXP Semiconductors**

E5.3 Optimal Order Polynomial Transformation for Calibrating Systematic Errors in Multisite Testing
***P. Farayola, I. Bruce, D. Chen*, Iowa State University*; A. Chaganti, A. Sheikh, S. Ravi*, Texas Instruments**

E5.4 Transforming an n-Detection Test Set into a Test Set for a Variety of Fault Models
***I. Pomeranz*, Purdue University**

E5.5 Improvements in the Automated IC Socket Pin Defect Detection
***V. Thangamariappan, N. Agrawal, C. C Xanthopoulos, J. Kim, I. Leventhal, K. Butler*, Advantest America*; J. Xiao*, Essai**

E5.6 GreyConE: Greybox Fuzzing + Concolic Execution Guided Test Generation for High Level Designs
M. Debnath, S. Sur-Kolay, Indian Statistical Institute; *A Chowdhury*, New York University; *D. Saha*, University of Calcutta

10:30 a.m. – 12:00 p.m. Pacific Daylight Time

SESSION A6
Special Session on Test of Quantum Circuits
J. Li, National Taiwan University
A6.1 Qubit fluctuations in quantum systems
M. Carroll, IBM
A6.2 Introduction to Quantum Circuit Testing (from Test Engineer's Perspective)
J. Li, National Taiwan University

SESSION B6
Scan-Based Learning and Diagnosis
W-T Cheng (Chair)
B6.1 Scan-Based Test Chip Design with XOR-based C-testable Functional Blocks
***Y-F. Chen,* Dept. EE, National Cheng Kung University; *D-Y. Kang,* Dept. EE, National Cheng Kung University; *K-J. Lee,* Dept. EE, National Cheng Kung University**
B6.2 Industry Evaluation of Reversible Scan Chain Diagnosis
***S. Urban, J. Janicki, M. Sharma, W-T. Cheng,* Siemens EDA; *M. Parley, K. Chung, S. Nicholson, S. Mittal,* Qualcomm**
B6.3 A Comprehensive Learning-Based Flow for Cell-Aware Model Generation
***P. d'Hondt,* LIRMM / STMicroelectronics; *A. Ladhar,* STMicroelectronics; *P. Girard, A. Virazel,* LIRMM**
B6.4 Runtime Fault Diagnostics for GPU Tensor Cores
***S. Hukerikar, N. Saxena,* NVIDIA**

SESSION C6
Special Session: Road to Chiplets: UCIe
Y. Zorian (Chair)
Presenters: *D. D. Sharma*, Intel, *Y. Zorian,* Synopsys. *K-D Hillinges, M. Braun,* Advantest

SESSION D6
Automotive II
C. He (Chair)
D6.1 Unsupervised Learning-based Early Anomaly Detection in AMS Circuits of Automotive SoCs
***A. Arunachalam, A. Kizhakkayil,* University of Texas at Dallas; *S. Kundu, K. Basu,* The University of Texas at Dallas; *A. Raha, S. Banerjee, F. Su,* Intel Corporation; *X. Jin,* NXP Semiconductors**
D6.2 Just-Enough Stress Test for Infant-Mortality Screening Using Speed Binning
***C-L. Tsai, S-Y. Huang,* National Tsing Hua University**
D6.3 Existence of Single-Event Double-Node Upsets (SEDU) in Radiation-Hardened Latches for Sub-65 nm CMOS Technologies
***M-H. Hsiao, P-T. Wang, C-W. Liang, H-P. Wen,* National Yang Ming Chiao Tung University**

SESSION E6
Industrial Practices III
K. Peng **(Chair)**
E6.1 Probeless DfT Concept for Testing 20k I/Os of an Automotive Micro-LED Headlamp Driver IC
***H. von Staudt,* Dialog Semiconductor - a Renesas Company; *L. Elnawawy,* Dialog Semiconductor, A Renesas Company; *S. Wang,* Dialog Semiconductor, A Renesas Company; *L. Ping,* Dialog Semiconductor, A Renesas Company; *J. Choi,* Samsung Electronics**
E6.2 Reusing IEEE 1687-Compatible Instruments and Sub-Networks over a System Bus
***F. Ghani Zadegan, Z. Zhang, K. Petersén,* Ericsson; *E. Larsson,* Lund University**
E6.3 Multi-die Parallel Test Fabric for Scalability and Pattern Reusability
***A. Sinha, Y. Cho, J. Easter, M. V. Leiva Rojas,* Intel**

1:30 p.m. – 3:00 p.m.

SESSION A7
Test Generation
S-K Lu (Chair)
A7.1 Compression-Aware ATPG
***X. Wang,* University of Chinese Academy of Sciences, Academy of mathematics and Systems Science; *Z. Wang,* HiSilicon Technologies Co., Ltd.; *N. Wang,* Hisilicon, Huawei; *W. Zhang,* HiSilicon Technologies Co., Ltd.; *Y. Huang,* Hisilicon, Huawei**
A7.2 DIST: Deterministic In-System Test with X-masking
***J. Tyszer, B. Wlodarczak,* Poznan University of Technology; *G. Mrugalski, J. Rajski,* Siemens Digital Industries Software**
A7.3 Test Generation for an Iterative Design Flow with RTL Changes
***J. Joe, I. Pomeranz,* Purdue University; *N. Mukherjee, J. Rajski,* Siemens Digital Industries Software**

SESSION B7
Low-Power and Test
H.-P. Wen (Chair)
B7.1 Understand VDDmin Failures for Improved Testing of Timing Marginalities
A. Singh, TU Delft
B7.2 ML-Assisted Vmin Binning with Multiple Guard Bands for Low Power Consumption
W-C. Lin, C-H. Hsieh, J-M. Li, C. Chen, National Taiwan University; *E-W. Fang,* MediaTek Inc.; *S-Y. Hsueh,* MediaTek inc.
B7.3 Comprehensive Power-Aware ATPG Methodology for Complex Low-power Designs
L. Manchukonda, E. Tsai, K. Abdel-Hafez,M. Dsouza, K. Natarajan, Synopsys; *S. Lai, W. Hsueh,* MediaTek

SESSION C7
Special Session: Design-for-Verification (DfV): A New Direction in Design Qualification
Y. Zorian (Organizer)
A. Majumdar (Moderator)
Presenter: *D. Akselrod,* AMD
Panelists:
S. Millican, Auburn University
S. Sunter, Siemens
A. Sharma, Synopsys
S. Huhn, University of Bremen

SESSION D7
Panel 4: Automotive Safety & Security Interoperability
Organizer: Nir Maor, QualComm
Moderator: Yervant Zorian, **Synopsys**

SESSION E7
Industrial Practices from ITC India
P. Wohl (Chair)

E7.1 TSV BIST Repair: Design-For-Test Challenges and Emerging Solution for 3D Stacked IC's
S. Akkapolu, Vaishnavi G, S. R. Malige, AMD

E7.2 Transfer-Matrix Abstractions to Analyze the Effect of Manufacturing Variations in Silicon Photonic Circuits
P. Agnihotri, P. Kalla, S. Blair, The University of Utah

E7.3 Selective Multiple Capture Test (SMART) XLBIST
P. Wohl, J. Waicukauski, V. Kumar K S, A. Bhat, R. Karmakar, Synopsys

Wednesday, 12:30 p.m. – 2:30 p.m. Pacific Daylight Time

PO.1 Neural Machine Translation for Test Language
S Go, SungKyunKwan University, Samsung Electronics

PO.2 Compositive Framework for Wafer Pattern Recognition with Confidence Relabeling Technique
L-Y Chen, Y-A Huang, C-S Lee, C-C Cheng, Y-Y Liao, L Chou J. Elwell, PNXP Semiconductors; *S-M Li,* National Sun Yat-Sen University; *S-J Wang,* National Chung Hsing University

PO.4 Teradyne's PortBridge Software Expedites Silicon Bring-Up, Debug, Production Readiness and Foundry Feedback
*R. Fanning,*Teradyne*; S. Molavi,* Broadcom

PO.5 Bridging Repairability Gaps in Shared Bus Architecture with Shared Physical Memory Implementation
W. Pradeep, N. Karkare; Google

PO.6 Design-for-Diagnosis for Multiple Defects per Chain
E. Gizdarski, Y. Kanzawa, Synopsys

PO.7 Roadblocks and Strategy to the Reuse of Test Solutions for Analog and Mixed-Signal Blocks
P. Bauwens, R. Vanhooren, A. Coyette, W. Dobbelaere, onsemi;*G. Gielen, N. Xama, J. Gomez,* KU Leuve

PO.8 Leveraging Existing High Speed Functional Serial Interfaces for Testing & Monitoring Silicon Throughout the Entire Lifecycle
R. Allen, A. Patel, Synopsys; *K. Hilliges,* Advantest; *B. Tully, A. Pandey,* Amazon

PO.9 Chiplet Level Test Parallelization for 3D Stacking Products
A. Margulis, T. Payakapan, J. Yuan, N.l Patel, A. Loh, AMD

PO.10 Pre-Analysis for ATPG Pattern Failures
D. Appello, D. Petrali, V. Tancorre, STMicroelectronics*; G. Chan, R. Dokken,* Roguevation

PO.11 Accelerating Design Cycle with DFT and Test Coverage Analysis at RTL
M. Arneson, Micron Technology; *R. Singhal, S. Nanduru,* Synopsys

PO.12 Prediction of Total Jitter using Machine Learning for LVDS Output Characterization
P. L. Lee, Intel

PO.13 Ehanced Jitter Reduction for Multi-GHz ATE
D. Keezer, Eastern Institute for Advanced Study; *D. Minier,* Boreas Technologies

PO.14 Deploying Real-Time Machine Learning Applications with Deep Data at Test
M. Hutner, A. Burlak, A. Mittall, proteanTecs

PO.15 HBM3 Test/Debug Solution Supporting PHY-Mastered Interface of HBMPHY
H. Son, Y. Lim, D. Han, Samsung Foundry

PO.16 Enabling a Low Cost and High Quality Scan Test Methodology in 16nm FinFet Automotive Products
S. Traynor, J. T. Ng, R. Chen., NXP Semiconductor

PO.17 Ultra-Fast and Secure 5G Digital Pre-Distortion with ACS Edge
D. Belkin, O. Olansky, Intel; *Y. Chen, K. Butler, K. Schaub,* Advantest

PO.18 IR-Drop Improvement with Packet-Based Scan
J. Reynick, Siemens EDA*; S. Alampally.,* Broadcom

PO.19 Investigation of Jitter Spur Impact on Eye Width Margin
O. Choong, W. C. Liew, Intel

PO.20 Improving Engineering Efficiency & Time to Market Through Multi-Variable Characterization
D. King, Galaxy Semiconductor

PO.21 Re-targeting Block-Level Patterns Using Top-Level On-Chip Clock Controller (OCC) --- An Industrial Case Study
Z. Zhong, S. Biswas, A. Wangoo, M. Bhattarai; Marvell Semiconductor Inc; *A. Gangwar,* Synopsys

PO.22 Identical HW and SW for producton test and lab validation of modules
F. Haas, and A. Matiz, ams-OSRAM

PO.23 Cell-Aware Test integration towards achieving 0 DPPB on automotive designs
N. K, S. Ramesh, R. Kaistha, J. K. Loh, G. S Clark, C. Ling, NXP Semiconductors

PO.24 A Novel Shift-left Method in Reducing Networking ASIC Customer Field DPM
K. A. Chuah, T. H. H. Tan, C. C. Tan, Intel

PO.25 Lcpll DTR: Recovering Yield Loss with Fusing and Graphics Driver
N. Wang-Lee, J. Abbas, K. L. Ng, H. Zhao, Y. Park, Intel

PO.26 An Application of Spatially Resolved Netlists to Graphical Error Detection
N. Taylor, J. Delozier, T. McDonley, K. Liszewski, B. Hayden, A. Kimura, Battelle Memorial Institute

PO.27 Low Cost, At-Speed Validation of I3C Target Design
P. Bansal, A. Bal, A. Kumari, STMicroelectronics

PO.28 ATE Integration of High Performance, High Data Rate 3rd Party Instruments
T. Lyons, Teradyne

PO.29 A Novel DFT [Design for Test] Clock Gating Technique to Reduce Power Consumption
A. Gangwar, F. Shukla, Synopsys; *S. Murthy, P. Policke,* Qualcomm

PO.31 Test Manufacturing Breakthroughs To Maximize Total Sellable Yield in 5G Network ASIC.
S. E. Wong, Intel

PO.32 A Breakthrough Manufacturing Solution - Array Erratic Fluctuation Predictive through Machine Learning Methods
N. H. Chun, T. Aik, Intel

PO.33 Advanced Core Wrapping for Power, Early Test Coverage and Automation
A. Gangwar, F. Shukla, K. Bachu, Synopsys

PO.34 Speedup Logic Diagnosis with Static Layout Data
R. Guo, Synopsys

PO.35 Design for test (DFT) Considerations when Designing Tile-based/abutted Physical Blocks
V. Neerkundar, Siemens

PO.36 Improving System Level Screening Efficiency Through Negative Voltage Margining
L.D. Rojas, J. Rodriguez, D. Wilhelmi, D. Lerner, Intel

PO.37 Built-In Self-Test architecture enabling diagnosis for massive Embedded Memory banks in large SoCs
G. Insinga, P. Bernardi, G. Paganini, A. Guerriero, Politecnico di Torino; *W. Mischo, R. Ullmann, M. Coppetta, G. Carnevale*, Infineon Technologies

Monday 4:30 p.m. – 6:00 p.m. PDT

Panel 1 – An Industry-wide Dialog on Chiplets and Heterogeneous Integration

Moderator: Phil Nigh

Panelists:

- Jeff Rearick – Chiplet Trends and Drivers
- Yervant Zorian – UCIe
- Ken Butler – HIR

Tuesday 4:00 p.m. – 5:30 p.m. PDT

Panel 2: Session A2: Are Last Century's Test Techniques Suitable for 21st Century Silent Errors?
Organizers: Sreejit Chakravarty, *Intel*
Subhashish Mitra, *Stanford University*
Moderator: Jeff Rearick*, AMD*
Panelists:

- Rama Govindaraju, *Google*
- Harish Dixit, *Meta*
- Pradeep Bose, *IBM*
- Sreejit Chakravarty, I*ntel*
- Subhasish Mitra, *Stanford*

Wednesday 4:30 p.m. – 6:00 p.m. PDT

Panel 3 – Session C5: Performing RAS in Today's Mission Critical Systems

Organizer: *Yervant Zorian,* Synopsys
Moderator: *Paolo Bernardi,* Polito Torino
Panelists:

- Rakesh Kinger, Google
- Nirmal Saxena, Nvidia
- Harish Dixit, Meta
- Yervant Zorian, Synopsys
- Dimitris Gizopoulos, Univ of Athens
- Prasanth Viswanathan Pillai, Texas Instruments
- ChunSheng Liu, Alibaba

Thursday 1:30 p.m. – 3:00 p.m. PDT

Panel 4 – Session D7: Automotive Safety & Security Interoperability
Organizer: Nir Maor, QualComm
Moderator: Yervant Zorian, Synopsys
Panelists:

- Sohrab Aftabjahani, Intel
- Luca Di Mauro, Arm
- Joytika Athavale, Nvidia
- Nir Maor, Qualcomm
- Jason M Fung, Intel
- Meirav Nitzan, Synopsys
- Thiyagu Loganathan, Infineon

IEEE Computer Society Test Technology Technical Council Workshops

Thursday and Friday

General Workshop Information

Two workshops are being held in parallel immediately following ITC 2022. They will each start with an opening address on Thursday afternoon, September 29, followed by a technical session. The remaining the technical sessions will be held on Friday, September 30. The technical scope of each workshop is described below.

Workshop Registration

All workshop participation requires registration. To register in advance for one of the workshops, do so online. Discount workshop registration rates apply until August 29, 2022. Workshop registration includes the opening address, technical sessions, and a digest of papers.

Workshop Schedule

The two workshops will adhere to the same schedule:

Thursday, September 29		Friday, September 30	
Plenary1, Keynote:	4:00 p.m. – 5:00 p.m.	Technical Sessions	8:00 a.m. – 4:00 p.m.
Technical Sessions:	5:00 p.m. – 6:30 p.m.		

Workshop Reception: Thursday September 29, 7:00 p.m. – 9:00 p.m.

Note: Workshop schedule is subject to change

Digest of Papers

A digest of papers will be distributed only to attendees at the workshops as an informal proceedings.

Further Information

For more information on the workshops contact their organizers by e-mail or check the TTTC Web site http://ieee-tttc.org

▪ ART 2022: IEEE Automotive Reliability and Test & Safety Workshop 2022

The ARTS workshop focuses exclusively on test, reliability and Safety of automotive and mission-critical electronics, including design, manufacturing, burn-in, system-level integration and in-field test, diagnosis and repair solutions, as well as architectures and methods for reliable and safe operations under different environmental conditions. With increasing system complexity, security, stringent runtime requirements for functional safety, and cost constraints of a mass market, the reliable operation of electronics in safety-critical domains is still a major challenge. This edition of the ARTS Workshop offers a forum to present and discuss these challenges and emerging solutions among researchers and practitioners alike.

Program Highlights:

- After the opening session of Thursday, Sundarrajan Subramanian , Qualcomm Vice President, will give the first Keynote speech on *"Journey from Mobile to Automobile: Leverage Learn Lead"* .
- Friday will start start with Vasanth Waran , Synopsys Senior Director, who will give the second Keynote speech on *"Evolution and Trends driving the Automotive Architecture and Ecosystems of the future"* .
- Four technical sessions will focus on:
    - *Advanced BIST design*
    - *NVM oriented reliability*
    - *In-field testing*
    - *Simulation and fault simulation techniques.*
- Technical sessions will be interleaved with a special session with a speech on "*The Accellera Functional Safety Standard: enabling automation, interoperability and traceability"* given by Alessandra Nardi , Accellera FS WG Chair.

See the ART2022 Web Page for full details on the ART Program.

General Chair: Yervant Zorian zorian@synopsys.com
Program Chair: Paolo Bernardi paolo.bernardi@polito.it
ART Web Page: http://art.tttc-events.org/

Second IEEE International Workshop on Silicon Lifecycle Management (SLM)

With increasing system complexity, security, stringent runtime requirements for functional safety, and cost constraints of a mass market, the reliable and secure operation of electronics in safety- critical, enterprise servers and cloud computing domains is still a major challenge. While traditionally design time and test time solutions were supposed to guarantee the in-field dependability and security of electronic systems, due to complex interaction of runtime effects from running workload and environment, there is a great need for a holistic approach for silicon lifecycle management, spanning from design time to in-field monitoring and adaptation. Therefore, the solutions for lifecycle management should include various sensors and monitors embedded in different levels of the design stack, access mechanisms and standards for such on-chip and in- system sensor network, as well as data analytics on the edge and in the cloud. The SLM Workshop offers a forum to present and discuss these challenges and emerging solutions among researchers and practitioners alike.

SLM include three keynote addresses and five technical sessions.
See the SLM Web Page for the complete SLM Program.

General Chair: Yervant Zorian zorian@synopsys.com
Program Chair: Mehdi Tahoori
SLM Web Page: https://people.rennes.inria.fr/Marcello.Traiola/SLM22/index.html

ITC 2022 is taking place the week of September 25-30, 2022. Attend in person to get the most out of the event and interact with presenters, exhibitors, and more. However, for those who cannot attend in person, we offer a virtual option, both for the main conference and for tutorials.

More details on what is available virtually will be provided later. Check the ITC website at itctestweek.org for the latest details.

Registration Categories

Register Online

All Test Week activities require a registration badge for admittance. There are three registration periods with differing fees

- Early discount preregistration through August 29, 2022
- Non-discount preregistration August 30 to September 24, 2022.

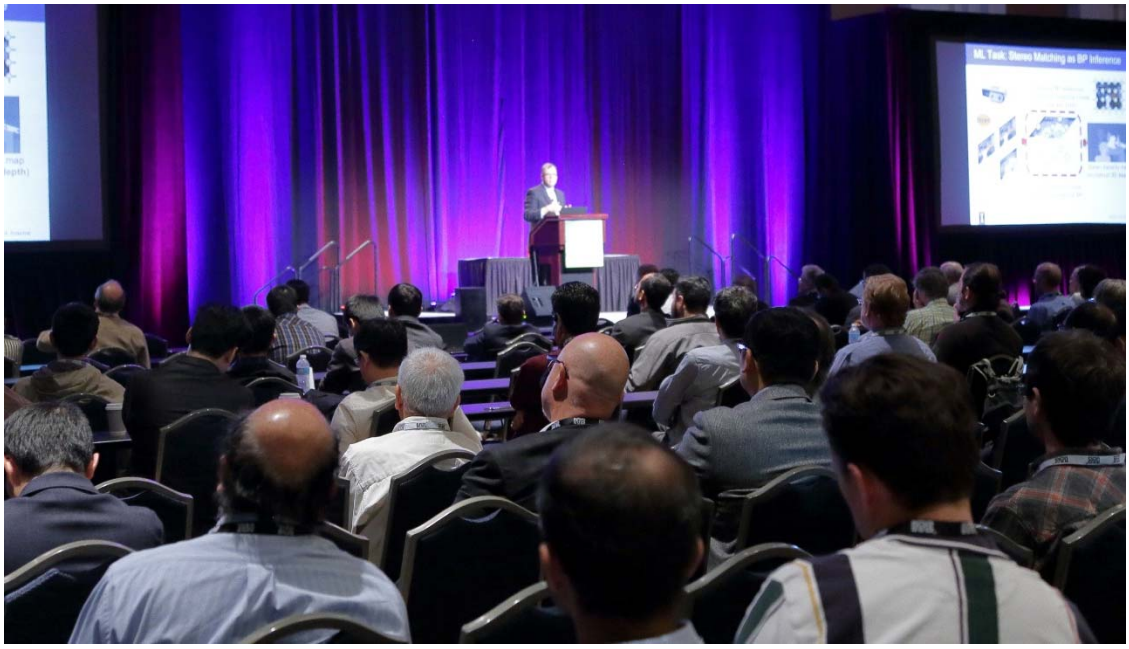
▶ITC Full-Conference Registration Includes ITC technical paper and panel sessions, exhibits, and access to ITC 2022 papers, slides and presentations for one month after the conference. Registration does not include the tutorials on Sunday and Monday or the workshops on Thursday and Friday.

▶Tutorial Registration Tutorials are a half-day in length.
One-Day tutorial registration fee is for two tutorials—a morning tutorial and afternoon tutorial, both on the same day, e.g., Tutorial 1 and Tutorial 4 on Sunday. You may register for up to four tutorials (two consecutive on Sunday and two consecutive on Monday).
All-Access Pass tutorial registration provides in-and-out access to all twelve tutorials over both days.

All registrations include study material, breaks and lunches on the day(s) attended. Tutorial registration does not include the ITC technical program, ITC receptions, exhibits, exhibit hall lunches, ITC publications, ITC giveaways or the workshops on Thursday and Friday.

▶Workshop Registration Includes the items specified on page 23. Registration does not include the ITC technical program, exhibits, or the tutorials on Sunday and Monday.

▶Discount Rates Early registration rates apply only when you complete your registration by August 29, 2022, either online or with a paper form and payment postmarked or faxed by August 29, 2022. To receive IEEE member or student member reduced rates, you must include your member number, which will be verified.



Registration Fees

Early Preregistration Rates (on or before September 2, 2022)

Early Discount Preregistration Fees	Full ITC Conf	One Day 2 Tutorials	All-Access Tutorial Pass	One Workshop
IEEE/CS Member	$795	$250	$490	$250
Nonmember	$994	$315	$615	$315
IEEE/CS Member, student or Life	$300	$225	$440	$225
Nonmember, student	$375	$285	$550	$285

Late Preregistration Rates (after September 2, 2022)

Late Preregistration Fees	Full ITC Conference	One Day 2 Tutorials	All-Access Tutorial Pass	One Workshop
IEEE/CS Member	$1050	$300	$580	$300
Nonmember	$1350	$375	$725	$375
IEEE/CS Member, student or Life	$300	$285	$560	$225
Nonmember, student	$375	$360	$710	$285

There are additional registration options for Program Participants, Virtual attendees. See http://www.itctestweek.org/register/ for full details.

Refunds

All refund/cancellation requests must be received in writing to registration+ITC@computer.org by **15 September 2022, 11:59 PM Eastern Time.** There will be an administrative fee of **US$10** for cancelled registrations

1. The ITC Advance Program release 2.1 was generated with Adobe Acrobat 8.2.6 on 16 September 2022

2. The program will be updated periodically as new material is available - check back often.

3. Navigate using the tabs and links at the top of each page.

4. Use underlined links in the At-a-Glance to find specific items.

5. For more information contact:

Subject	Contact	Email
Advance Program	Scott Davidson	davidson.scott687@gmail.com
Corporate Forum	Chen-huang Chiang	chen-huan.chiang@intel.com
Exhibits and Exhibiting	Chen-huang Chiang	chen-huan.chiang@intel.com
Fringe Technical Meetings	IEEE Computer Society	ieeeitc@computer.org
Posters	KJ Lee	kjlee@mail.ncku.edu.tw
Registration	IEEE Computer Society	ieeeitc@computer.org
Technical Program	KJ Lee	kjlee@mail.ncku.edu.tw
TTTC Tutorials	Yervant Zorian	zorian@synopsys.com
TTTC Workshops	Yervant Zorian	zorian@synopsys.com
All Other Questions	IEEE Computer Society	ieeeitc@computer.org

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