ITC 2021 Final Program

ITC Welcome Message

It is our privilege to welcome you to the 52nd International Test Conference (ITC) sponsored by IEEE and the IEEE Philadelphia Section. ITC is the world's premier conference dedicated to electronics test.

Our volunteer committees have worked very hard to put together an exciting event with a balance of the latest research and practical techniques related to electronics test. As we continue to deal with the coronavirus pandemic, and taking the safety of all participants into consideration, we have once again moved ITC Test Week events to a fully online format with shorter days to maximize the opportunity to attend from home or the office without any travel being required.

This year's program looks at a variety of traditional and emerging areas of test. Themes such as Test Infrastructure (including talks about security hardware, analog hardware, and automotive considerations), Test Diagnosis (including talks about AI and wafer map classification) and Enhancing Test (including talks about reducing test patterns and higher quality testing for automotive) are in the main tracks of the conference. Safety, Security, Memory Testing and Trusted Electronics will also be featured in standalone sessions and tutorials. AI hardware, machine learning, data analysis, and their relationship to test will also continue to be highlighted in the program. Multiple panels are scheduled, and posters will be present in the online exhibit hall, with an opportunity to talk directly to poster presenters during a pre-scheduled session.

Exciting keynotes by industrial leaders will be presented at the beginning of each day of the conference. These keynotes cover a variety of timely topics, including advanced semiconductor memories, technology innovation, and silicon lifestyle management. On Wednesday and Thursday, the keynote will be followed by a visionary talk from academia exploring aspects of AI and machine learning in the context of EDA or the Sport Technology Industry.

The Thursday keynote is a natural prelude to the beginning of the 1st IEEE International Workshop on Silicon Lifecycle Management (SLM)—starting on Thursday afternoon and continuing into Friday. Simultaneously, the 6th IEEE Workshop on Automotive Reliability, Test and Safety will commence—once again exploring multiple aspects of this critical area of electronic test.

ITC is also continuing its expanded presence! For the fifth year, in 2021 there were ITC-India and ITC-Asia conferences held in July and August respectively. We have included two sessions with the best three papers from ITC-Asia and ITC-India.

The traditional exhibition floor has been replaced with online exhibition "booths". Solutions providers will be available for discussion and learning about their offerings, and one-on-one meetings will be easy to arrange. A corporate forum is held online and merged into the program, where exhibiting companies present about their products.

This year's virtual conference, tutorials, and workshops will also benefit from enhanced online networking capabilities that will enable participants to easily meet and talk on the virtual exhibit floor and "outside" in both public and private conversational spaces. Presenters will also be available in clearly identified areas on the exhibit floor for post-presentation discussions. Please make sure to visit the exhibit hall in between sessions to connect with exhibitors, customers, and colleagues during all of the conference breaks.

On behalf of the 2021 International Test Conference steering committee, the program committee and all of the dedicated volunteers who are key to making the program complete, we welcome you to this year's exciting technical program and exhibits.

Jennifer Dworak
General Chair

Teresa McLaurin
Program Chair

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	Sunday	Monday	Tuesday	Wednesday	Thursday	Friday
12 Half-Day TTTC Tutorials A great way to prepare for the ITC Technical program	●	●				
Four Panels			●	●	●	
Plenary Sessions, 3 Keynotes, 2 Visionary Talks			●	●	●	
66 Technical Presentations			●	●	●	
Three Tracks: Test Infrastructure, Test Diagnosis and Enhancing Test			●	●	●	
World-Class Exhibits Virtual Exhibit Booths			●	●	●	
Corporate Forum The latest technical innovations from our exhibitors and corporate supporters			●	●		
Posters				●		
Two-Day Workshops Two to choose from					●	●
Virtual Meeting Rooms	●	●	●	●	●	●

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SUNDAY, OCTOBER 10 – HALF-DAY TUTORIALS			
8:00 a.m. – 11:00 a.m.	Tutorial 1 Safety and Security in Automtive 2.0 Era	Tutorial 2 Testing and Monitoring of Die-to-Die Interconnection in a 2.5D/3D IC	Tutorial 3 AI Chip Technologies and their DFT Methodologies
12:00 p.m. – 3:00 p.m.	Tutorial 4 Machine Learning in Data Analytics	Tutorial 5 Mixed-Signal DFT and BIST: Trends, Principles and Solutions	Tutorial 6 Power-Aware Testing in the Era of IOT

MONDAY, OCTOBER 11 – HALF-DAY TUTORIALS			
8:00 a.m. – 11:00 a.m.	Tutorial 7 Silicon Lifecycle Management for Emerging Memories	Tutorial 8 Applications of Machine Learning in Semiconductor Manufacturing and Test	Tutorial 9 Scan Test Escapes, New Fault Models and Effectiveness of Functional System Level Tests
12:00 p.m. – 3:00 p.m.	Tutorial 10 Automotive Functional Safety, Reliability and Test Solutions	Tutorial 11 SOC Security Verification	Tutorial 12 From Test to Post-Silicon Validation: Concepts and Recent Trends

TUESDAY, OCTOBER 12 – TECHNICAL SESSIONS				
8:00 a.m. – 9:00 a.m.	Plenary – Opening Session Keynote**: Future Prospects of Semiconductor Memories --- Advancements and Challenges**. Chih-Yuan Lu, President, *Macronix International Corp.*, Chairman and CEO, *Ardentec Corp*.			
9:00 a.m. – 9:30 a.m.	Coffee Break and Exhibits			
9:30 a.m. – 10:30 a.m.	Session 1A Enhancing Testability	Session 1B ML for Diagnosis	Session 1C Special Session: Start to Finish: 2.5D and 3D Device Testing Challenges and Solutions	Session 1D ITC-Asia 2021 Top 3 Papers
10:30 a.m. – 11:00 a.m.	Coffee Break and Exhibits			
11:00 a.m. – 12:00 p.m.	Diamond Supporter Presentation			
12:00 p.m. – 1:00p.m.	Session 2A AI Hardware	Session 2B Wafer Map Classification I	Session 2C Special Session: STT-MRAMs: Technology, Design and Test	Session 2D TTTC McCluskey PhD Competition
1:00 p.m. – 2:00 p.m.	Meal Break and Exhibits			
2:00 p.m. – 3:00 p.m.	Panel 1: SLT - What is it today? Why is it needed?		Panel 2: What is the best high-speed I/O Test Method: 1149.10 or high speed I/O protocol?	
3:00 p.m. – 4:30 p.m.	External event: TTTC's Global Test Community Quiz			

All Times are Pacific Daylight Time

WEDNESDAY, OCTOBER 13 – TECHNICAL SESSIONS				
8:00 a.m.–9:00 a.m.	Plenary Session Keynote: **Refusing Limits in Technology Innovation**, *Ron Nersesian. President and CEO, Keysight* Visionary Talk: Machine Learning and Corpus Design for EDA and Beyond, *Roger Jang, Prof. NTU, CTO, E.Sun Financial Holding Company*			
9:00 a.m. – 9:30 a.m.	Coffee Break and Exhibits			
9:30 a.m.–10:30 a.m.	Session 3A Security Hardware	Session 3B Wafer Map Classification II	Session 3C Current Developments in Test Standards	Session 3D ITC-India 2021 Top 3 Papers
10:30 a.m.–11:00 a.m.	Coffee Break and Exhibits			
11:00 a.m-12:00 pm	Corporate Forum			
12:00 p.m.–1:00p.m.	Session 4A Secure and Trusted Microelectronics	Session 4B Failure Diagnosis	Session 4C Test Enhancements	Session 4D ET1: Memory Testing Embedded Tutorial
1:00 p.m.–2:00p.m.	Meal Break and Exhibits			
2:00 p.m.–3:00 p.m.	Panel 3: Talk to the TTSC (Test Technology Standard Committee)			
2:00 p.m.–3:30 p.m.	Posters			

THURSDAY, OCTOBER 14– TECHNICAL SESSIONS				
8:00 a.m – 9:00 a.m.	Plenary Session Keynote: **Addressing Design Challenges in the Era of SysMoore: From Architecture to Silicon Lifecycle Management**, *Shankar Krishnamoorthy, SVP, Synopsys* Visionary Talk: Sport Technology Industry: A New Frontier for AI, 5G and Semiconductor, *Cheng-Wen Wu, NTHU*			
9:00 a.m – 9:30 a.m	Coffee Break and Exhibits			
9:30 a.m.–10:30 a.m.	Session 5A Circuits and Monitors	Session 5B Test Data	Session 5C Test Architecture and Infrastructure	Session 5D Accellera FuSa WG
10:30 p.m. – 11:00 a.m.	Coffee Break and Exhibits			
11:00 a.m – 12:00 p.m.	Exhibits & Networking			
12:00 p.m.–1:00 p.m.	Session 6A What's Going on With 1687*?	Session 6B Analog Testing	Session 6C Automotive FuSa Tolerance	Session 6D Silicon Lifecycle Challenges
1:00 p.m.– 2:00 p.m.	Meal Break and Exhibits			
2:00 p.m.– 3:00 p.m.	Panel 4: Challenges of 3rd party IPs to achieve Automotive Zero Defect quality and Functional Safety			

THURSDAY, OCTOBER 14 – WORKSHOPS		
3:30 p.m. – 5:00 p.m.	6th IEEE Workshop on Automotive Reliability, Test and Safety Plenary1: Opening, Keynote	1st IEEE Intl Workshop on Silicon Lifecycle Management (SLM) Plenary1: Opening, Keynote

8:00 a.m. – 3:00 p.m.	6th IEEE Workshop on Automotive Reliability, Test and Safety	1st IEEE Intl Workshop on Silicon Lifecycle Management (SLM)

Test Infrastructure **Test Diagnosis** **Enhancing Test**

All times are Pacific Daylight Savings Time

TTTC TEST TECHNOLOGY EDUCATION PROGRAM (TTEP) 2021

The Tutorials & Education Group of the IEEE Computer Society Test Technology Technical Council (TTTC) organizes a comprehensive set of Test Technology Tutorials to be held in conjunction with several TTTC-sponsored technical meetings worldwide. The mission of the Test Technology Educational Program (TTEP) is to serve test and design professionals by offering fundamental education and expert knowledge in state-of-the-art test technology topics. TTEP offers tutorial participants the opportunity to earn official certification from IEEE Computer Society TTTC. Each half-day tutorial corresponds to two TTEP units. Upon completion of 16 TTEP units, official recognition in the form of an IEEE TTTC Test Technology Certificate will be presented to the participant. For further information regarding TTEP, please visit http://ttep.tttc-events.org/ttep/index.html

At ITC 2021, TTTC/TTEP is pleased to present 12 **half-day tutorials** on topics of current interest to test professionals and researchers. All tutorials qualify for credit towards IEEE TTTC certification under the TTEP program. Six tutorials are held on Sunday, October 10. Six tutorials will be held on Monday, October 11.
The **one-day** tutorial registration fee is for two tutorials—a morning tutorial and afternoon tutorial, both on the same day, e.g., Tutorial 1 and Tutorial 4 on Sunday. You may register for up to four tutorials (two consecutive tutorials on Sunday and two consecutive tutorials on Monday).
The **all-access pass** tutorial registration provides in-and-out access to all twelve tutorials over both days.
(see registration page or http://www.itctestweek.org for further information).

Sunday 8:00 a.m. – 11:00 a.m. PDT

TUTORIAL 1
Safety and Security in the Automotive 2.0 Era

Presenters: V. Prasanth, S. Ravi

Increasing semiconductor consumption has been spurred by a revolution witnessed in the automotive industry. The integration of electronics and networking into conventional automobiles driven by infotainment and ADAS a few years back is accelerated by megatrends of EV/HEV, autonomous driving and shared mobility. These trends, termed sometimes as *Automotive 2.0*, drive various requirements into the semiconductors being sourced. Of these, safety and security requirements are becoming paramount due to their impact and liability from failures. This tutorial leverages the authors' experiences in driving safety and security as a part of semiconductor development cycles. By breaking down complex system requirements into foundational ones at semiconductor level, the tutorial is intended to provide an accessible treatment of the subject for any semiconductor developer.

TUTORIAL 2
Testing and Monitoring of Die-to-Die Interconnects in a 2.5D/3D IC

Presenter: S-Y Huang

With the evolution of multi-die integration into the era of interposer- or InFO-based 2.5-D ICs and/or TSV-based 3D stacked ICs, die-to-die interconnects could operate in a very high speed, with an end-to-end delay of only a few hundreds of picoseconds. Parametric defects (like small delay faults, resistive open/bridging faults, leakage faults, etc.) have been identified as potential threats to the yield and reliability of a 2.5D/3D IC product. Fortunately, various test and online monitoring methods have been developed to deal with this challenge and to guarantee the overall quality of the die-to-die interconnects in a 2.5D/3D IC product.
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TUTORIAL 3
AI Chip Technologies and DFT Methodologies

Presenters: L. Harrison, P. Orlando, Jay Jahangiri, G. Eide

In this tutorial, we will start by covering the basics of deep learning. We will proceed to give an overview of the new and exciting field of using AI chips to accelerate deep learning computations. It will cover the critical and special characteristics and the architecture of the popular AI chips. Next, we will summarize the features of the AI chips from design-for-test (DFT) perspective and introduce the DFT technologies that can help testing AI chips. Finally, we will present a few case studies on how DFT is implemented in the real AI chips. In this tutorial, we will present some of the functional and structural monitoring techniques that are available today for automotive ICs. An overall architecture showing how functional and structural monitoring can be implemented will also be presented.

Sunday 12:00 p.m. – 3:00 p.m. PDT

TUTORIAL 4
Machine Learning in Data Analytics

Presenter: L-C. Wang, Chuanhe (Jay) Shan

Applying "machine learning" (ML) in data analytics has received growing interest in recent years. Analysis of "data" originated from design and test processes has been a common practice in the semiconductor industry for decades, well before the modern ML became a hot topic. What are the potential added values brought by the modern ML to the existing data analytics practices in design and test? The first part of the tutorial provides a review of the basic principles for applying ML in selected applications and highlights gaps for achieving a deployable ML solution. The second part introduces the idea of Intelligent Engineering Assistant (IEA), designed to enable ML to be applied in a real-world application. Key technologies for implementing an IEA agent will be discussed. In principle, an IEA agent is an AI software system incorporating human perception in its analytics. Results based on actual industrial settings will be presented and discussed.

TUTORIAL 5
Mixed-Signal DFT and BIST: Trends, Principles and Solutions

Presenter S. Sunter

This tutorial explores systematic analog design for test and analog fault simulation, especially for automotive ICs. We review trends in ad hoc DfT, fault simulation, IEEE 1149.1/4/6/7/8/10 (briefly), 1687, and ISO26262, then BIST for ADC/DAC, PLL, SerDes/DDR, and random analog. Essential principles of practical analog BIST are presented, then practical DfT techniques, from quicker analog defect simulation, to over/under sampling methods that improve range, resolution, and reusability. We conclude with a discussion of the Analog Defect Coverage and Test Access standards (P1687.2, P2427), and measurement of ISO 26262 metrics.

TUTORIAL 6
Power-Aware Testing in the Era of IoT

Presenters: P. Girard, X. Wen

Managing power consumption of circuits is among the most important challenges for the semiconductor industry in the IoT era. Dedicated techniques are used to control the power dissipation during functional operation. As these techniques have profound implications on manufacturing test, power-aware testing has become indispensable for low-power IoT devices. This tutorial provides a comprehensive coverage of power-aware testing. The first part gives background and discusses power issues during test. The second part provides comprehensive information on structural and algorithmic solutions for alleviating test-power problems. The third part shows how low-power devices can be tested safely without affecting yield and reliability.

Monday 8:00 a.m. – 11:00 a.m. PDT

TUTORIAL 7
Silicon Lifecycle Management for Emerging Memories

Presenter: Y. Zorian

Recent growth in artificial intelligence and content delivery has led to an explosion in the use of emerging memories, from on-chip 3nm FinFET SRAMs, CAMs, MRAMs; to off-chip DDR and HBM DRAMs in chiplets and 3DIC solutions. This tutorial will start with the trends and challenges of these emerging memories throughout their lifecycle, from manufacturing to in-field utilization, and then will move to the solution space by addressing the health of such emerging memories: from initial self-test, debug, and self-repair; to periodic reliability sensing and transparent BIST; and constant error correction, safety and security monitoring and on-chip/off-chip data analytics.

TUTORIAL 8
Applications of Machine Learning in Semiconductor Manufacturing and Test

Presenters: H. Stratigopolos, Y. Makris

Throughout the lifetime of an integrated circuit, a wealth of data is collected for ensuring its reliable operation. Ranging from design-time simulations to process characterization monitors, and from high-volume specification tests to diagnostic measurements on customer returns, the information inherent in this data is invaluable. Mining this information using machine learning methods has seen intense interest and numerous breakthroughs during the last decade. This tutorial seeks to elucidate the utility of machine learning in semiconductor manufacturing and test. Relevant concepts from machine learning will be introduced, agglomerated with current practice, and showcased using industrial data. Recommendations for practitioners will also be given.

TUTORIAL 9
Scan Test Escapes, New Fault Models, and the Effectiveness of Functional Level System Tests

Presenter: A. Singh

This tutorial aims at understanding the increasing use of functional system level tests (SLTs) as an additional final defect screen before processor SOCs are shipped for assembly. For this, we take an in-depth look at traditional scan based Stuck-at and TDF tests to understand potential sources of test escapes. We also extensively discuss the effectiveness of new test generation methodologies such as Cell Aware, Gate Exhaustive, Transistor Stuck-Open, and Timing Aware in plugging these structural test holes. Based on this, we identify failures that can still remain undetected by low cost scan structural tests, and require the use of expensive functional SLTs to achieve desired defect levels. In conclusion, we suggest strategies to minimize use SLTs without impacting defect levels.

Monday 12:00 p.m. – 3:00 p.m. PDT

TUTORIAL 10
Automotive Functional Safety, Reliability and Test Solutions

Presenters: R. Mariani, Y. Zorian

Given today's fast-growing automotive semiconductor industry, this tutorial will discuss the implications of automotive quality, functional safety, and reliability on all aspects of automotive SOC lifecycle, while accelerating time to market for these semiconductor ICs. The automotive SOC lifecycle stages will include design, silicon bring-up, volume production, and particularly in-system operation. Today's automotive safety critical chips need multiple in-system modes, such as power-on and power-off self-test and repair (key-on/key-off), periodic in-field self-test during mission mode, advanced error correction solutions, etc. This tutorial will analyze these specific in-system test modes and the discuss the benefits of using ISO 26262 including its second edition, and several newer standardization efforts, in order to ensure that standardized functional safety requirements are met.

TUTORIAL 11
SoC Security Verification

Presenters: M. Tehranipoor, F. Farahmandi

The growing complexity of system-on-chips (SoCs) and the increased security requirements have made security verification a major challenge. It is imperative to develop security verification solutions as well as automatic CAD tools to identify and detect such vulnerabilities at pre-silicon while it is possible to change the design and address security vulnerabilities. The goal of this tutorial is to present (i) vulnerabilities introduced during various stages of the design life cycle, (ii) CAD tools and methodologies for security assessment, (iii) Countermeasure tools and methodologies for addressing each vulnerability, and (iv) challenges and research roadmap ahead.
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TUTORIAL 12
From Test to Post-Silicon Validation: Concepts and Recent Trends

Presenters A. Sinha, S. Ray

The tutorial provides a broad overview of post-silicon bring-up, debug, and diagnosis, and discusses fundamental concepts and current practices. It introduces the spectrum of validation activities, e.g., functionality, software compatibility, electrical characteristics, speed path, etc. Activities involved in validation planning along the system life cycle and various conflicts and trade-offs are discussed. The trade-offs span a spectrum of topics, including security, power management, and physical design. The tutorial will describe approaches to repurpose Design-for-Test (DFT) infrastructure for post-silicon validation, and the collaboration areas between validation and test. Instrumentation, control, and observability technologies including tracing and triggering, scan and array dumping, and off-chip transport will be addressed. The focus of the tutorial is on industrial adoption and practice.

ITC Exhibitors*

Esteemed:

Siemens

Synopsys, Inc.

Regular:

STAr Technologies

TSSI

** As of publication date*

The ITC Virtual Exhibit Hall is Open whenever technical sessions are not meeting, and at other times by appointment.

Corporate Forum/TTTC Global Test Community Quiz

The Corporate Forum track provides an opportunity for ITC exhibitors and supporters to present information on their latest products and services.

The **Corporate Forum** will be held from 11:00 am – 12:00 pm PDT on Wednesday, October 13. All times are **Pacific Daylight Time**.

Day	Time	Company	Title of Presentation
Tuesday	11:00 am	Siemens	Our commitment to innovation – what's next for Streaming Scan Network
Wednesday	11:00 am	Siemens	A Novel Reversible Scan Chain Technology that Improves Chain Diagnosis Resolution by 4X
Wednesday	11:15 am	Synopsys	Manufacturing Test and Silicon Lifecycle Management
Wednesday	11:45	STAr Technologies, Inc.	STAr – the Semiconductor Test Architect
Wednesday	11:50	TSSI	TSSI VirtualTest Saves Weeks in ATE Patterns Bring-up

TTTC's Global Test Community Quiz during ITC TestWeek 2021 – External Event

The Global Test Community Quiz (GTCQ) is a free 'must-attend' social event for everyone in the world-wide test community. The next edition will be organized on Tuesday October 12, 2021, 3:00-4:30pm PDT as online social event during the 52nd IEEE International Test Conference (ITC) 2021. Participation to this entertaining fun event is free and open not only to all registered attendees of ITC-2021, but to all members of the global test community.
For logistical reasons, free registration is required at this website of EventBrite: https://www.eventbrite.com/e/tttcs-global-test-community-quiz-gtcq-at-itc-2021-tickets-177474911237.

Tuesday 8:00 a.m. – 9:00 a.m.

Opening Remarks
Jennifer Dworak, *ITC 2021 General Chair*

ITC 2021 Program Introduction
Teresa McLaurin, *ITC 2021 Program Chair*

ITC 2020 Paper Awards Presentation
Jennifer Dworak, *ITC 2020 Program Chair*

TTTC Awards Presentation
Yervant Zorian

Keynote Address

Future Prospects of Semiconductor Memories – Advancement and Challenges

Chih-Yuan (C. Y.) Lu *President, Macronix International Corp; Chairman and CEO, Ardentec Corp.*

Semiconductor memories embrace a bright future in this big data era. The recent global pandemic challenges essentially accelerate the human society toward the 4th generation of industrial revolution of digital life augmented with smart devices. The fast evolution of AI, 5G, automotive, data center, cloud, and edge intelligent devices for IoT all trigger more market demands in semiconductor memories. SRAM, DRAM and Flash are classic standard semiconductor memories, and we believe that these classic memories will continue tremendous momentum to improve the technology with ever better performances, power, and cost. On the other hand, new emerging memories and new emerging computing architectures have potential to create new paradigms. Memory devices will become the central role during data processing, and emerging computing architecture such as computing-in-memory (CIM) or in-memory search (IMS) will complement the conventional computing architectures to create disruptive applications. Memory devices will continue to improve the memory density and bandwidth performances, while reliability is always the major priority to ensure the memory quality. We observe obvious increased complexities in the wafer sort (WS) and final test (FT) for advanced memory technologies, and we would encourage the society to conceive more advanced and even intelligent testing methods to support advanced memory technologies. Co-optimizations between processing, design, testing, and memory controllers must help to manage the large tuning parameters to adapt to production variations to ensure the high quality of memory products with affordable cost.
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About the speaker: Chih-Yuan Lu received B.S. degree from *National Taiwan University*, and Ph.D. degree in physics from *Columbia University*, NYC. Dr. Lu has been a professor in *National Chiao-Tung University,* and with *AT&T Bell Labs*.; later he joined *ERSO/ITRI* in 1989 as a Deputy General Director responsible for the *MOEA grand Submicron Project.* This project successfully developed Taiwan the first 8-inch manufacturing technology with high density DRAM/SRAM, and thus led Taiwan semiconductor industry onto world stage. He was therefore granted the *National Science & Technology Contribution Award* by Taiwan Prime Minister, due to his leadership and achievements in this *Submicron Project*.
Dr. Lu was the co-founder, and later the President of *Vanguard International Semiconductor Corp.*, which was the spin-off memory IC Company from *ITRI* with Taiwanese technology independency. In late 1999, Dr. Lu founded *Ardentec Corp.*, he now is the Chairman and CEO of *Ardentec Corp.* a global hidden champion type VLSI testing company. CY also served *Macronix International* as CTO, SVP, and now as its President. Dr. Lu led *Macronix'*s technology development and product teams to successfully establish the state-of-the-art non-volatile memory technology, and led its overall operation. CY's leadership and technology excellency make *Macronix* as a top player in non-volitile memory field with high quality and strong IP positions.
Dr. Lu is also a *Distinguished Chair Professor* in *National Taiwan University, also as NTU's Distinguished Alumni*. Due to his seminal contributions to semiconductor technology and achievements in IC industry, he was granted the *Honorable Doctorate Degree* from *National Chiao-Tung University;* and the highest life honor from *ITRI* as "*ITRI Laureate".*
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8:00 a.m. – 8:30 a.m.

Refusing Limits in Technology Innovation

Ron Nersesian *President and CEO, Keysight*

More reach. More data. Longer battery life. Today's engineers are constantly rethinking what's possible in a world where everyone, and everything, is connected. Not only has the pace of integration accelerated, but today's designs also do more, with less resources. Leading-edge disruptive innovations don't come without pushing the limits of what's technically possible and making difficult tradeoffs.

In this session, Ron Nersesian, CEO for Keysight Technologies, will share examples of the trends and challenges we see customers innovate through every day, and how software automation and AI will become key to breaking through the limits coming next.

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About the speaker: Ron Nersesian is chairman, president, and chief executive officer of Keysight Technologies. In November 2011, he was named executive vice president and chief operating officer of Agilent Technologies. The following year, in November 2012, he was promoted to president and chief operating officer.

When Agilent announced the separation of its electronic measurement business in 2013, Nersesian was appointed Keysight president and CEO and led the launch of the new company. Keysight became a public, independent company in November 2014. Nersesian was appointed chairman of Keysight in 2019.

Nersesian began his career in 1982 with Computer Sciences Corporation as a systems engineer for satellite communications systems. In 1984, he joined Hewlett-Packard and served in a range of management roles during his tenure. In 1996, Nersesian joined another industry player as vice president of worldwide marketing. He subsequently assumed other senior management roles through 2002, including senior vice president and general manager of the company's digital storage oscilloscope business.

Nersesian joined Agilent Technologies in 2002 as vice president and general manager of the company's Design Validation Division. In 2005, he was named vice president and general manager of the company's Wireless Business Unit and manager of Agilent's Santa Rosa, California site. In 2009 Nersesian was named president of Agilent's Electronic Measurement Group.

Nersesian holds a bachelor's degree in electrical engineering from Lehigh University and an MBA from New York University, Stern School of Business. He also serves as a member of Georgia Tech's Advisory Board.

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8:00 a.m. – 8:30 a.m.

Title: Addressing Design Challenges in the Era of SysMoore: From Architecture to Silicon Lifecycle Management

Shankar Krishnamoorthy *General Manager Digital Design Group, Corporate Staff, Synopsys*

Abstract: The amount of compute power required in today's SoCs, especially in AI applications, is outpacing Moore's Law by a wide margin. Orders of magnitude compute are needed to keep pace with this new era of scaling and system complexity, otherwise known as the SysMoore era. In this presentation we examine the challenges driving the next wave of innovative design solutions. Starting with architecture exploration to silicon-lifecycle management, these solutions will help engineers create designs that keep pace with the compute power and silicon health needs for today and tomorrow.

About the speaker Shankar is the general manager of the Digital Design Group, responsible for the digital design platform including synthesis, signoff analysis, place-and-route, test automation, and formal verification solutions. Most recently, he served as senior vice president of the Digital Implementation Group, delivering several game-changing innovations including Fusion Compiler, RTL Architect, 3DIC Compiler, TestMAX solutions. Shankar has more than 25 years of experience leading world-class teams that have delivered the industry's premier IC physical design and logic synthesis solutions.

Before rejoining Synopsys in 2017, he was at Mentor Graphics where he served as general manager of the IC Design Solutions Division. He joined Mentor in 2007 as part of the acquisition of Sierra Design Automation, where he was the founder and CTO. Prior to Sierra Design, Shankar led Synopsys' Physical Synthesis and Logic Synthesis R&D organizations. He began his career at Synopsys in 1992 working on logic synthesis technology.

Shankar received his M.S. in Computer Science from the University of Texas, Austin in 1992, and his bachelor's degree in Technology and Computer Science from the Indian Institute of Technology, Bombay in 1990

Wednesday, October 13
8:30 a.m. – 9:00 a.m.

Machine Learning and Corpus Design for EDA and Beyond

Jyh-Shing Roger Jang, *National Taiwan Univ. (NTU), CTO E.Sun Financial Holding Company*

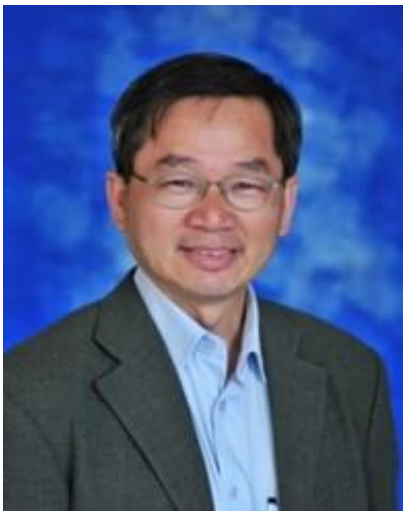
We have been building faster computers to host innovative ML (machine learning) applications such as image recognition and language understanding. But can we reverse the roles and use ML to help EDA (electronic design automation) to create better performing chips and computers? The answer is definitely yes. In this talk, we shall cover two such examples, including wafer failure analysis and side channel attacks using ML. Actually, these two examples only scratch the surface since there are a number of ML tasks for EDA to produce better computers for advanced ML applications. We believe such positive feedback in the loop will advance both ML technologies as well as chip/computer performance. Moreover, we shall also address the guidelines for ML corpus design, and touch on corpus-hungry ML applications that outperform humans by a large margin and were unthinkable before the current AI era.

About the Speaker: Jyh-Shing Roger Jang received Ph.D. from EECS Department at UC Berkeley, where he studied fuzzy logic and neural networks with Lotfi Zadeh, the father of fuzzy logic. As of July 2021, Google Scholar shows over 18,000 citations for Dr. Jang's seminal paper on ANFIS published in 1993. After obtaining his Ph.D., he joined the MathWorks to coauthor the Fuzzy Logic Toolbox (for MATLAB). He has since cultivated a keen interest in implementing industrial software for machine learning. He was a professor in the CS Dept. of National Tsing Hua Univ., Taiwan, from 1995 to 2012. Since August 2012, he has been a professor in the CSIE Dept. of National Taiwan Univ. (NTU), Taiwan. He served as the IT director for NTU Hospital during 2017-2019, and the director for FinTech Center at NTU during 2018-2020. He is currently serving as CTO of E.Sun Financial Holding Company at Taipei. His research focuses on machine learning in practice, with wide applications to speech recognition/assessment/synthesis, music analysis/retrieval, image classification, medical/healthcare data analytics, and FinTech.

Thursday, October 14
8:30 a.m. – 9:00 a.m.

Sport Technology Industry: A New Frontier for AI, 5G, and Semiconductor

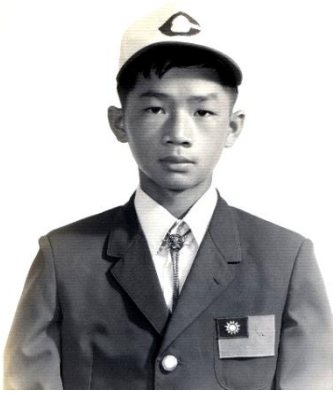
Cheng-Wen Wu *National Tsing-Hua University, Taiwan,.Senior Vice President, ITRI, Taiwan, Chief Advisor, Center for Sport Technology, NTHU, Taiwan*



I will introduce the new semiconductor opportunities in the fast-growing sport industry that is being populated and renovated by emerging technologies. The sport industry is much larger than the semiconductor industry itself. Development of sport technology requires cross-disciplinary research and education in the sport domain and the technology side, i.e., in addition to the domain knowledge in sport science, we need to integrate technologies in IOT, AI, 5G, cloud computing, advanced sensors, etc. Trends in areas like *smart venue*, *immersive media*, *quantified athlete*, *e-sport*, *real-time online streaming*, *fan engagement*, etc., will be introduced. Examples of existing products, systems, and services powered by semiconductors will be given, and future directions that calls for *innovative semiconductor design and test technologies* will be addressed.

About the speaker.

- Pitcher and short stop in Taiwan's National Little League Baseball Team (the Tainan Giants),and won the 1971 Little League World Series in Williamsport, Pennsylvania, USA.
- Pitcher and short stop of the NTU Baseball Team—won the 1981 Championship in the National University Series (Category 2—non-baseball specialty students).
- BS in EE, National Taiwan University (NTU), 1981.
- MS/PhD in ECE, UCSB, 1985/1987.
- Joined Dept. EE, NTHU in 1988.Served at NTHU as the Director of Computer Center, Chair of EE Dept., Director of IC Design Technology Center, Dean of the College of EECS, and Senior Vice President for Research.



9:30 a.m. – 10:30 a.m. PDT

SESSION 1A
Enhancing Testability
V. Chickermane, Cadence (Chair)

1A.1 A Fast and Low Cost Embedded Test Solution for CMOS Image Sensors
J. Lefevre, P. Debaud, STMicroelectronics; *P. Girard*, LIRMM / CNRS; *A. Virazel*, LIRMM

1A.2 ACE-Pro: Reduction of Functional Errors with ACE Propagation Graph
D-A. Yang, Y-T. Chang, T-S. Hsu, J-J. Liou, National Tsing Hua University; *H. Chen*, MediaTek Inc.

1A.3 Testability-Enhancing Resynthesis of Reconfigurable Scan Networks
N. Lylina, C-H. Wang, H-J. Wunderlich, University of Stuttgart

SESSION 1B
ML for Diagnosis
K. Butler, Advantest (Chair)

1B.1 Machine Learning for Circuit Aging Estimation under Workload Dependency
F. Klemme, H. Amrouch, University of Stuttgart

1B.2 Adaptive NN-based Root Cause Analysis in Volume Diagnosis for Yield Improvement
X. Huang, M. Qin, R. Xu, S. Jui, Z. Ding, Y. Huang, Huawei; *C. Chen*, National Taiwan University; *P. Li*, University of California, Santa Barbara

1B.3 Minimum Operating Voltage Prediction in Production Test Using Accumulative Learning
Y-T. Kuo, C. Chen, C-H. Hsieh, W-C. Lin, J-M. Li, National Taiwan University; *E-W. Fang, S-Y. Hsueh*, MediaTek inc.

SESSION 1C
Special Session: Start to Finish: 2.5D and 3D Device Testing Challenges and Solutions
M. Keim, Siemens *(Chair)*

1C.1 Moderator Introduction
J. Rearick, AMD

1C.2 3DIC Test Challenges, Trends and Solutions - an EDA perspective
W. Yang, Siemens

1C.3 Designing and testing 3D devices – A fabless company perspective
Y. Heo, Samsung

1C.4 Testing challenges and solutions for advanced packaging technologies - A foundry perspective
S. Goel, TSMC

Test Infrastructure

SESSION 1D
ITC-Asia 2021 Top 3 papers
G. Qu, University of Maryland (Chair)

1D.1 Smart Sampling for Efficient System Level Test: A Robust Machine Learning Approach
C. Lu J. Ou, Huawei

1D.2 The Security Enhancement Techniques of the Double-layer PUF Against the ANN-based Modeling Attack
Y. Chen X. Cui, W. Ye, X. Cui, Peking University

***1D.3* Software-Based Self-Test for Transition Delay Faults in Pipelined Processors**
J-L. Huang, National Taiwan University

12:00 p.m. – 1:00 p.m.

SESSION 2A
AI Hardware
K. Chakravadhanula, Cadence (Chair)

2A.1 On-line Functional Testing of Memristor-mapped Deep Neural Networks using Backdoored Checksums
C-Y. Chen, K. Chakrabarty, Duke University

2A.2 Efficient Fault-Criticality Analysis for AI Accelerators using a Neural Twin
A. Chaudhuri, C-Y. Chen, J. Talukdar, S. Madala, K. Chakrabarty, Duke University; *A. Dubey*, Oak Ridge National Laboratory

2A.3 Efficient Functional In-Field Self-Test for Deep Learning Accelerators
Y. He, Y. Li, University of Chicago; *T. Uezono*, Hitachi Ltd.

Test Diagnosis

SESSION 2B
Wafer Map Classification I
K. Shu-Min Li, National Sun Yat-Sen University *(Chair)*

2B.1 Wafer-level Variation Modeling for Multi-site RF IC Testing via Hierarchical Gaussian Process
M. Shintani, R-U. Mian, M. Inoue, NAIST; T. Nakamura, M. Kajiyama, M. Eiki, Sony Semiconductor Manufacturing Corporation

2B.2 Brain-Inspired Computing for Wafer Map Defect Pattern Classification
P. Genssler, H. Amrouch, University of Stuttgart

2B.3 Semi-supervised Wafer Map Pattern Recognition using Domain-Specific Data Augmentation and Contrastive Learning
H. Hu, University of California, Santa Barbara; C. He, NXP Semiconductors; P. Li, University of California, Santa Barbara

SESSION 2C
Special Session: STT-MRAMs: Technology
A. Gebregiorgis, Delft University of Technology *(Chair)*

2C.1 STT-MRAM Technology for Embedded Applications
S. Rao, IMEC

2C.2* Design of Reliable Sensing Mechanisms in *STT-MRAMs
M. Tahoori, Karlsruhe Institute of Technology

2C.3 Device-Aware Test for STT-MRAM
S. Hamdioui. Delft University of Technology

SESSION 2D
TTTC McCluskey PhD Competition
M. Portolan, TIMA (Chair)

2D.1 Study on High-Accuracy and Low-Cost Recycled FPGA Detection
F. Ahmed, M. Shintani, M. Inoue, Nara Institute of Science and Technology

2D.2 Testing STT-MRAM: Manufacturing Defects, Fault Models, and Test Solutions
L. Wu, M. Taouil, S. Hamdioui, Delft University of Technology

2D.3 Adaptive Methods for Machine Learning-Based Testing of Integrated Circuits and Boards
M. Liu, K. Chakrabarty, Duke University

Enhancing Test

9:30 a.m. – 10:30 a.m. Pacific Daylight Time

SESSION 3A
Security Hardware
S. Blanton, Carnegie Mellon *(Chair)*

3A.1 Impeccable Circuits III
S. Rasoolzadeh, Radboud University; A. Rezaei Shahmirzadi, A. Moradi, Ruhr University Bochum

3A.2 A BIST-based Dynamic Obfuscation Scheme for Resilience against Removal and Oracle-guided Attacks
J. Talukdar, K. Chakrabarty, Duke University; S. Chen, Carnegie Mellon University; A. Das, AMD; S. Aftabjahani, Intel Corporation; P. Song, IBM T.J. Watson Research Center

3A.3 LL-ATPG: Logic-Locking Aware Test Using Valet Keys in an Untrusted Environment
M. Rahman, H. Li, R. Guo, F. Rahman, F. Farahmandi, M. Tehranipoor, University of Florida

SESSION 3B
Wafer Map Classification II
A. Gattiker, IBM (Chair)

3B.1 Triplet Convolutional Networks for Classifying Mixed-Type WBM Patterns with Noisy Labels
C. Liu, Q. Tang, Huawei Technology Ltd

3B.2 Semi-Supervised Framework for Wafer Defect Pattern Recognition with Enhanced Labeling
L-Y. Chen, X-H. Jiang, A-A. Huang, NXP Semiconductors Taiwan Ltd.; *K-M. Li, S-J. Wang,* National Chung Hsing University; *J. Chen,* National Central University; *H-C. Liang,* CYCU; *C-L. Hsu,* Industrial Technology Research Institute

3B.3 MINiature Interactive Offset Networks for Wafer Map Classification
Y. Zeng, L-C. Wang, University of California Santa Barbara; *C. Shan,* IE3A, Inc.

SESSION 3C
Current Development in Test Standards.
I. McIntosh TTTC (Chair)

3C.1 Revisions to IEEE Std 1500, Standard Testability Method for Embedded Core-based Integrated Circuits
M. Ricchetti, Synopsys

3C.2 Update on the development of P1687.1, extending IEEE 1687 for non-TAP Interfaces
M. Laisne., Dialog Semiconductor

3C.3 Assisting board level connectivity test with IEEE Std 1581
H. Ehrenberg, GOEPEL Electronics

SESSION 3D
ITC-India 2021 Top 3 Papers
R. Parekhji, Texas Instruments ***(Chair)***

3.D.1 Targeting Zero DPPM through Adoption of Advanced Fault Models and Unique Silicon Fall-out Analysis
A. Acharya, N. Naresh, P. Narayanan, R. Parekhji, K. Roush, H. Ibarra, R. Sheth, C. Flora, W. Pradeep, Texas Instruments

3.D.2 Addressing High Speed Memory Interface Test Quality Gaps in Shared Bus Architecture
W. Pradeep, R. Gottumukkala, S. Vooka, Google

3.D.3 A Novel Method to measure PLL Bandwidth in a 5G RF transceiver
P. Nair, D. A, Texas Instruments

12:00 p.m. – 1:00 p.m.

SESSION 4A
Secure and Trusted Microelectronics
Y. Iskander, Microsoft (Chair)

4A.1 Characterizing Corruptibility of Logic Locks using ATPG
D. Duvalsaint, S. Blanton, Carnegie Mellon University

4A.2 SymbA: Symbolic Execution at C-level for Hardware Trojan Activation
A. Vafaei, M. Tehranipoor, F. Farahmandi, University of Florida; *N. Hooten,* Dynetics

4A.3 Security and Provisioning of Automotive IC's through Test and Safety
L. Harrison, Siemens

SESSION 4B
Failure Diagnosis
S. Adham, TSMC (Chair)

4B.1 Improving Volume Diagnosis and Debug with Test Failure Clustering and Reorganization
M-T. Wu, C-S. Kuo, J-M. Li, National Taiwan University; *C. Nigh,* Carnegie Mellon University; *G. Bhargava,* Qualcomm Technologies, Inc.

4B.2 Relevant Signals and Devices for Failure Analysis of Analog and Mixed-signal Circuits
T. Melis, Univ. Grenoble Alpes, CNRS; *E. Simeu,* TIMA Laboratory; *L. Saury,* STMicroelectronics; *E. Auvray,* Fastnet Technologies

4B.3 Open-short Normalization Method for a Quick Defect Identification in Branched Traces with High-resolution Time-domain Reflectometry
Y. Shang, Advantest (Singapore) Pte Ltd; *M. Shinohara, E. Kato, M. Hashimoto,* Advantest Corporation; *J. Kiljan,* Qualcomm, Inc

SESSION 4C
Test Enhancements
H. Walker, Texas A&M (Chair)

4C.1 On Reduction of Deterministic Test Pattern Sets
J. Tyszer, Poznan University of Technology; *J. Rajski, S. Milewski, S. Eggersgluess,* Siemens Digital Industries Software

4C.2 Multi-Transition Fault Model (MTFM) ATPG patterns towards achieving 0 DPPB on AUTOMOTIVE designs
J. Corso, S. Ramesh, K. Abishek, L. Tan, C. Lew, NXP Semiconductors

4C.3 Analyzing and Mitigating Sensing Failures in Spintronic-based Computing in Memory
M. Mayahinia, C. Münch, M. Tahoori, KIT University

SESSION 4D
ET1: Memory Testing Embedded Tutorial
Benoit Nadeau-Dostie, Siemens (Chair)

Presentations:

1. **Memory BIST requirements -** *Raghav Mehta*, Siemens EDA
2. **Memory repair -** *Benoit Nadeau-Dostie,* Siemens EDA
3. **eMRAM test challenges and MBIST support -** *Jongsin Yun*, Siemens EDA

:

9:30 a.m. – 10:30 a.m. Pacific Daylight Time

SESSION 5A
Circuits and Monitors
J. Carulli, GlobalFoundries (Chair)

5A.1 Revisit to Accurate ADC Testing with Incoherent Sampling Using Proper Sinusoidal Signal and Sampling Frequencies
K. Sato, T. Ishida, T. Okamoto, T. Ichikawa, ROHM Semiconductor; *J-L. Wei, T. Nakatani, Y. Zhao, S. Katayama, S. Yamamoto, A. Kuwana, K. Hatayama, H. Kobayashi*, Gunma University

5A.2 Adaptive High Voltage Stress Methodology to Enable Automotive Quality on FinFET Technologies
S. Traynor, K. Klein, Y. Yu, NXP; *C. He*, NXP Semiconductors

5A.3 3.5Gsps MIPI C-PHY Receiver Circuit for Automatic Test Equipment
S. Lee, M. Kang, C. Park, H. Ryu, J. Choi, B. Yim, Samsung Electronics

5A.4 A Scalable Design Flow for Performance Monitors Using Functional Path Ring Oscillators
T. Kilian, Infineon Technologies AG, Technical University of Munich; *H. Ahrens, D. Tille*, Infineon Technologies AG; *M. Huch*, Infineon Technology AG; *U. Schlichtmann*, Technical University of Munich

SESSION 5B
Test Data (Short Papers)
P. Song, IBM (Chair)

5B.1 WGrid: Wafermap Grid Pattern Recognition with Machine Learning Techniques
P-Y. Liao, L-Y. Chen, A-A. Huang, K-C. Cheng, C-Y. Tsai, L. Chou, NXP Semiconductors Taiwan Ltd.; *K-M. Li, S-J. Wang*, National Chung Hsing University

5B.2 AAA: Automated On-ATE AI Debug of Scan Chain Failures
C. Nigh, R. Blanton, Carnegie Mellon University; *G. Bhargava*, Qualcomm Technologies, Inc.

5B.3 Systematic Hardware Error Identification and Calibration for Massive Multisite Testing
P. Farayola, I. Bruce, D. Chen, Iowa State University; *S. Chaganti, A. Obaidi, A. Sheikh, S. Ravi*, Texas Instruments

5B.4 Low Power Shift and Capture through ATPG-Configured Embedded Enable Capture Bits
Y. Sun, H. Jiang, L. Ramakrishnan, T. Manikas, J. Dworak, Southern Methodist University; *K. Nepal*, University of St. Thomas; *I. Bahar*, Brown University

SESSION 5C
Test Architecture and Infrastructure
F. Su, Intel (Chair)

5C.1 Is your secure test infrastructure secure enough? Attacks based on delay test patterns using transient behavior analysis
S. Meschkov, Institute of Computer Engineering, Karlsruhe Institute of Technology (KIT); *D. Gnad*, Institute of Computer Engineering, Karlsruhe Institute of Technology (KIT); *J. Krautter*, Institute of Computer Engineering, Karlsruhe Institute of Technology (KIT); *M. Tahoori*, KIT university

5C.2 Seamless Physical Implementation of ASIC Hierarchical Integrated Scan Architecture
B. Suparjo, J. Chetia, A. Shah, Intel Corporation

5C.3 Testability-Aware Low Power Controller Design with Evolutionary Learning
M. Li, Z. Shi, Q. Xu, The Chinese University of Hong Kong; *Z. Wang*, Huawei Technologies Co., Ltd.; *W. Zhang*, Huawei Technologies Co., Ltd.; *Y. Huang*, Huawei

5C.4 An automated formal-based approach for reducing Undetected faults in ISO26262 hardware compliant designs
F. Augusto da Silva, A. Bagbaba, C. Sauer, Cadence Design Systems; S. Hamdioui, Delft University of Technology

SESSION 5D
Accellera FuSa WG: Automation, Interoperability and Traceability in Functional Safety Standardization
Moderators: *Alessandra Nardi*, Cadence; *Nir Maor*, Qualcomm
Discussants:
Prasanth Viswanathan Pillai, Texas Instruments
Kaushik De, Synopsys
Bala Chavali, AMD

12:00 p.m. – 1:00 p.m.

SESSION 6A
What's going on with 1687*?
M. Ricchetti, Synopsys (Chair)

6A.1 Security EDA Extension through P1687.1 and 1687 Callbacks
M. Portolan, V. Reynaud, P. Maistri, R. Leveugle, G. Di Natale, TIMA Laboratory

6A.2 Accessing General IEEE Std. 1687 Networks via Functional Ports
E. Larsson, P. Murali, Z. Zhang, Lund University

6A.3 IEEE P1687.1 Data Retargeting and Transformations for Accessing Internal Cores
M. Laisne, H. M. von Staudt, Dialog Semiconductor; *A. Crouch*, Amida; *M. Keim*, Siemens; *M. Portolan*, TIMA; *J. Rearick*, AMD; *B. Van Treuren*, VT Enterprises; *S. Zuo*, Tailored Management

SESSION 6B
Analog Testing
S. Sunter, Siemens (Chair)

6B.1 Summing Node and False Summing Node Methods: Accurate Operational Amplifier AC Characteristics Testing without Audio Analyzer
D. Iimori, T. Nakatani, S. Katayama, G. Ogihara, A. Hatta, A. Kuwana, J. Wei, Y. Zhao, T. Tran, K. Hatayama, H. Kobayashi, Gunma University; *K. Sato, T. Ishida, T. Okamoto, T. Ichikawa*, ROHM Semiconductor

6B.2 Automatic Verification of Mixed-Signal ATE Test Programs using Device Variation
F. Mayer, C. Schott, E. Billich, S. Yazdani, U. Heinkel, Chemnitz University of Technology; *G. Daler, B. Ruf, R. Pannuzzo, W. Dickenscheid*, Infineon Technologies AG

6B.3 Background Receiver IQ Imbalance Correction for in-Field and Post-Production Testing and Calibration
M. Avci, S. Ozev, Arizona State University

SESSION 6C
Automotive FuSa Tolerance
W. Dobbelaere, On Semiconductor (Chair)

6C.1 Exploiting Application Tolerance for Functional Safety
P. Viswanathan Pillai, Texas Instruments; *R. Parekhji*, Texas Instruments (Bangalore); *B. Amrutur*, Indian Institute of Science

6C.2 Hierarchical Failure Modeling and Machine Learning Assisted Correction of Subsystem Failures in Autonomous Vehicles
C. Amarnath, M. Momtaz, A. Chatterjee, Georgia Institute of Technology

6C.3 Compositional Fault Propagation Analysis in Embedded Systems using Abstract Interpretation
C. Bartsch, D. Stoffel, W. Kunz, University of Kaiserslautern; *S. Wilhelm, D. Kästner*, AbsInt Angewandte Informatik GmbH

SESSION 6D
Silicon Lifecycle Challenges
Yervant Zorian, Synopsys (Chair)

6D.1 Silent Data Corruptions at Scale
Harish Dattatraya Dixit, Sneha Pendharkar, Matt Beadon, Chris Mason, Tejasvi Cahkravarthy, Bharath Muthiah, Sriram Sankar, Facebook Inc.

6D.2 Cores that don't count
Peter H. Hochschild, Paul Turner, Jeffrey, C. Mogul, Rama Govindaraju, Parthasarathy Ranganathan, David E. Culler, Amin Vahdat, Google

6D.3 A Software Solution for Managing Silicon Defects in Data Centers
Arjan van de Ven, Ian M. Steiner, Intel Corp

Wednesday, 2:00 p.m. – 3:30 p.m. Pacific Daylight Time

PO.1 Understanding Tool Synthesis Behavior and Safe Finite State Machine Design
T. McDonley, K. Liszewski, A. Kimura, Battelle Memorial Institute

PO.2 Generalized Insider Attack Detection Implementation using NetFlow Data for Distributed Test Range Networks
Y. Samtani, Ridge High School; *J. Elwell,* Perspecta Labs

PO.3 FR4 could be better than Tachyon-100G for post-silicon validation on LVDS signaling
P. Lee, Intel

PO.4 Defect-Directed Stress Testing Using I-PAT Inline Defect Inspection Results
C. He, P. Grosch, O. Anilturk, J. Witowski, C. Ford, R. Kalyan, NXP Semiconductors; *J. Robinson, D. Price, J. Rathert, B. Saville,* KLA Corporation

PO.5 Layout Informed Multiple Bit Upset Hardening of Finite State Machines
T. McDonley, J. Delozier, K. Liszewski, A. Kimura, Battelle Memorial Institute

PO.6 Power-Aware ATPG Using Sign-Off Models
W. Hsueh, S. Lai, MediaTek; *K. Abdel-Hafez, A. Cron,* Synopsys

PO.7 In-Field Embedded Sensing & PVT Monitoring for Increased Device Power and Performance Optimization
R. Allen, Synopsys

PO.8 Jitter Injection with pre- and post- emphasis circuits
T. Mak, L. Ungar, N. Jacobson, A T E Solutions

PO.9 A Novel Fault Grading Technique to Establish RTL-ATPG Top-Off Coverage
K. Adebo, E. Brazil, S. Pillai, Intel; *F. Shukla, P. Mahajan, H. Eriksson,* Synopsys

PO.10 Unified Test Flow for DFT Power, Performance & Area Optimization
TS. Duggirala, R. Singhal, Synopsys

PO.11 A Multi-Threaded Single-Pass Diagnosis of Scan Chain Failures
E. Gizdarski, Y. Kanzawa, Synopsys

PO.12 High Bandwidth Current Sourcing with the Howland Current Source
D. Marsh, Teradyne, Inc.

PO.13 Practical Methods to Test MIPI C-Phy Data Interfaces
T. Lyons, Teradyne Inc

PO.14 Utilizing IEEE Std 1687 for board level test
H. Ehrenberg, N. Muench, T. Wenzel, GOEPEL Electronics LLC

Tuesday 2:00 p.m. – 3:00 p.m. PDT

Panel 1 - SLT - What is it today? Why is it needed?

Organizer/Moderator: *Phil Nigh*

Panelists: *Harry Chen*, Mediatek; *Sajjad Pagarkar*, Google; *Davide Appello*, ST Microelectronics; *John Yi*, AMD; *Paul Maccoux*, Intel

The panelists will discuss a series of topics about SLT such as:

- After all the ATE/structural testing done -- why is SLT needed?
- Is SLT done broadly for 100% of products? Or is it only done on sample?
- Is the use growing or staying steady?
- Does SLT only focus on adding functional test content? Or are people adding a lot of structural tests?
- How does ATE Final Test change if SLT is done?
- How do SLT requirements change for different applications? High end processors. Data Centers / AI / ML Mobile processors Auto ICs –
- System-level perspective -- how to enable component SLT to deliver higher quality systems?

Panel 2: What is the best high-speed I/O Test Method: 1149.10 or high speed I/O protocol?

Organizers: *Ramsay Allen/Robert Ruiz*, Synopsys

Moderator: *Anne Meixner*

Panelists: *Claudia Bertani*, ST Microelectronics, *Klaus-Dieter Hilliges*, Advantest-Europe, *Steve Pateras*, Synopsys

Because shorter digital test time with an increasingly limited number of pins is a constant goal for manufacturing test, various high test bandwidth methods have been deployed with others in the final stages of development. While ad-hoc methods, such as using serializing-deserializing techniques, were coming online, the IEEE 1149.10 standard appeared. The standard defines a common high-speed interface for greater digital test bandwidth (especially for scan patterns), but practical considerations regarding physical implementation could potentially inhibit its deployment. On the other hand, functional high-speed interfaces, with defined protocols already exist for functional data could be reused for test data, but no standard exists for such applications. What are the advantages and disadvantages of using IEEE 1149.10 vs functional high-speed I/O such as USB and PCIe? Are there any other competing high-speed I/O techniques? What are the practical considerations for any such solution? And, how soon will DFT teams need to consider using a highspeed I/O for test data?

Wednesday 2:00 p.m. – 3:00 p.m. PDT

Panel 3 - Talk to the TTSC (Test Technology Standard Committee)

Organizer: *Mike Ricchetti*
Moderator: *Jeff Rearick*

Rather than a traditional panel, this will be an interactive session in which the audience can ask questions of the Test Technology Standards Committee members, and even make requests and provide feedback and guidance. Likewise, the TTSC members could survey the audience as well.

Thursday 2:00 p.m. – 3:00 p.m. PDT

Panel 4: Challenges of 3rd party IPs to achieve automotive zero-defect quality and functional safety

Organizer and Moderator: *Chen He,* NXP

Panelists: *Davide Appello*, ST Microelectronics; *Wim Dobbelaere*, ON Semiconductor; *Fei Su*, Intel; *Daniel Tille,* Infineon; *Jody Defazio*, Synopsys; *John Xu*, Xscend Technology

The advent of autonomous driving as well as the switch towards electric cars are causing a continuous growth of the electronic content in modern vehicles. As a result, automotive semiconductor manufacturers are demanded to meet Zero Defect (ZD) quality level as well as Functional Safety (FuSa) requirements. Testing and stressing to screen out potential early life failures caused by extrinsic defects is crucial to ensure ZD quality. However, screening defects is only as good as the test and stress coverage enabled in the design. Design for ZD needs to be addressed at both IP level and SOC/SIP (system on chip/system in package) level. As the technology feature size keeps scaling down, the design complexity has increased exponentially. Driven by cost and time-to-market considerations, it has become more and more popular for automotive semiconductor suppliers to adopt the off-the-shelf 3rd party IPs on their SOC/SIPs. This, however, poses unique challenges on ZD testing and stressing due to the lack of automotive ZD stress/test requirements built in the 3rd party IPs as well as the lack of the detailed design knowledge of those IPs from the system integration point of view. Adding manufacturing test flow awareness to the DFT/stress guidelines followed by IP providers is not straightforward. Information about how transforming provided fault coverage achievements into actual test coverage is not part of the typical IP utilization guidelines. Consequently we have seen cases in which the 3rd -party IP were not tested or stressed sufficiently resulting in quality issues as well as cases in which the 3rd -party IPs were overstressed and caused qualification failures. Meanwhile, FuSa is usually considered at the system level, not at the IP level. Moreover, for different FuSa integrity levels, we may need different stress testing requirements. How to ensure the 3rd party IP designs meet FuSa requirements while achieving ZD quality in a systemic and holistic way has become a common but important challenge faced by the automotive semiconductor industry. It is important to clearly define the requirements for IP providers before the design starts and make sure they have the effectively access to all necessary inputs regarding to the ZD quality and FuSa objectives. In this panel, experts in this field will exchange their views and discuss possible solutions and remaining challenges on this important topic.

IEEE Computer Society Test Technology Technical Council Workshops

Thursday and Friday

General Workshop Information

Two workshops are being held in parallel immediately following ITC 2021. They will each start with an opening address on Thursday afternoon, October 14, followed by a technical session. The remaining the technical sessions will be held on Friday, October 15. The technical scope of each workshop is described below.

Workshop Registration

All workshop participation requires registration. To register in advance for one of the workshops, do so online. Discount workshop registration rates apply until September 12, 2021. Workshop registration includes the opening address, technical sessions, and a digest of papers.

Workshop Schedule

The two workshops will adhere to the same schedule:

Thursday, October 14		Friday, October 15	
Plenary1, Keynote:	3:30 p.m. – 5:00 p.m.	Technical Sessions	8:00 a.m. – 3:00 p.m.

Note: Workshop schedule is subject to change

Digest of Papers

A digest of papers will be distributed only to attendees at the workshops as an informal proceedings.

Further Information

For more information on the workshops contact their organizers by e-mail or check the TTTC Web site http://ieee-tttc.org

- **ART 2021: IEEE Automotive Reliability and Test & Safety Workshop 2021**

The ARTS workshop focuses exclusively on test, reliability and Safety of automotive and mission-critical electronics, including design, manufacturing, burn-in, system-level integration and in-field test, diagnosis and repair solutions, as well as architectures and methods for reliable and safe operations under different environmental conditions. With increasing system complexity, security, stringent runtime requirements for functional safety, and cost constraints of a mass market, the reliable operation of electronics in safety-critical domains is still a major challenge. This edition of the ARTS Workshop offers a forum to present and discuss these challenges and emerging solutions among researchers and practitioners alike.
ARTS will take place in conjunction with the IEEE International Test Conference (ITC 21); is sponsored by IEEE Philadelphia Chapter; and conceived by the IEEE Test Technology Technical Council (TTTC).

Highlights from 2021 ART2021 include:

- Thursday keynote by Antonio Priore, ARM
- Friday keynote by Davide Santo, STM
- Sessions on
  - In-field reliability and hardware security
  - EDA tools and testing technologies
  - AI approaches for automotive systems safety
- Special session on FuSA

General Chair: Yervant Zorian zorian@synopsys.com
Program Chair: Paolo Bernardi paolo.bernardi@polito.it
ART Web Page: http://cas.polito.it/ART2021/

1st IEEE International Workshop on Silicon Lifecycle Management (SLM)

With increasing system complexity, security, stringent runtime requirements for functional safety, and cost constraints of a mass market, the reliable and secure operation of electronics in safety-critical, enterprise servers and cloud computing domains is still a major challenge. While traditionally design time and test time solutions were supposed to guarantee the in-field dependability and security of electronic systems, due to complex interaction of runtime effects from running workload and environment, there is a great need for a holistic approach for silicon lifecycle management, spanning from design time to in-field monitoring and adaptation. Therefore, the solutions for lifecycle management should include various sensors and monitors embedded in different levels of the design stack, access mechanisms and standards for such on-chip and in-system sensor network, as well as data analytics on the edge and in the cloud. This inaugural edition of the SLM Workshop tries to build a community around this topic and offer a forum to present and discuss these challenges and emerging solutions among researchers and practitioners alike.
SLM will take place in conjunction with the IEEE International Test Conference (ITC 21), it is sponsored by IEEE Philadelphia Chapter and conceived by the IEEE Test Technology Technical Council (TTTC).

Highlights from SLM include:

- Thursday keynote by Rich Bonderson, Google
- Friday keynote by Ravi Iyer, University of Illinois
- 15 great papers, including ones on:
  - System telemetry
  - Extracting added value from test
  - Malware detection
  - … and many more
- Panel on **"The silicon lifecycle management ecosystem at large"**

General Chair: Yervant Zorian zorian@synopsys.com
Program Chair: Mehdi Tahoori

SLM Web Page: https://inl.cnrs.fr/events/slm2021/

Virtual ITC

ITC 2021 is taking place virtually the week of October 10-15, 2021. Attend live to get the most out of the event and interact with presenters, exhibitors, and more.

After you register for ITC you will receive an email from Underline, our virtual conference providers, with a link that will allow you to create a password for the Underline system. Once the Virtual ITC site is available, logging into Underline will provide you with a link that will allow you to enter ITC. Links to tutorials on how to use the system will be made available on the ITC website before the conference begins.

If you do not have time to attend LIVE during the week of the conference please read below as there will be content available On-Demand through the end of day (ET) November 16th, 2021.
Recorded videos of the following conference content will be accessible after the conference and until November 16th, 2021:

- Plenary sessions, including keynote speeches
- 24 technical presentation sessions, organized in 4 parallel tracks
- ART and SLM workshops presentations
- Posters

The following content is LIVE only and will not be available after the scheduled event time:

- TTTC tutorials
- Panels

During ITC TestWeek, October 10-15, 2021, ITC will run several types of sessions, including Live Presentations, Video Presentations, Panels, and Posters.

- Plenary sessions are presented live, where keynote speeches are presented live with live Q&A
- Technical papers are presented with pre-recorded video and with live Q&A
- Panels are live discussions
- Posters are presented with individual pages including a recorded introductory video and a break-out room for discussion
- Tutorials and workshops are presented live.

Please note that during the conference a pre-recorded technical paper presentation video will be played only during the time slot allocated. A session chair will moderate the session and the audience can ask questions at the end of the presentation and at the end of the session (during the break time).

Registration Categories

Register Online

All Test Week activities require a registration badge for admittance. There are three registration periods with differing fees

- Early discount preregistration through September 12, 2021
- Non-discount preregistration September 13 to October 14, 2021.

▶ITC Full-Conference Registration Includes ITC technical paper and panel sessions, exhibits, and access to ITC 2021 papers, slides and presentations for one month after the conference. Registration does not include the tutorials on Sunday and Monday or the workshops on Thursday and Friday.

▶Tutorial Registration Tutorials are a half-day in length.
One-Day tutorial registration fee is for two tutorials—a morning tutorial and afternoon tutorial, both on the same day, e.g., Tutorial 1 and Tutorial 4 on Sunday. You may register for up to four tutorials (two consecutive on Sunday and two consecutive on Monday).
All-Access Pass tutorial registration provides in-and-out access to all twelve tutorials over both days.

All registrations include study material, breaks and lunches on the day(s) attended. Tutorial registration does not include the ITC technical program, ITC receptions, exhibits, exhibit hall lunches, ITC publications, ITC giveaways or the workshops on Thursday and Friday.

▶Workshop Registration Includes the items specified on page 23. Registration does not include the ITC technical program, exhibits, or the tutorials on Sunday and Monday.

▶Discount Rates Early registration rates apply only when you complete your registration by September 12, 2021, either online or with a paper form and payment postmarked or faxed by October 12, 2020. To receive IEEE member or student member reduced rates, you must include your member number, which will be verified.

Registration Fees

Early Preregistration Rates (on or before September 12, 2021)

Early Discount Preregistration Fees	Full Conference	One Day 2 Tutorials	All-Access Tutorial Pass	One Workshop
IEEE/CS Member, Non-author	$180	$80	$120	$80
Nonmember, non-author	$225	$100	$150	$120
IEEE/CS Member, author	$400	$80	$120	$80
Nonmember, author	$500	$100	$150	$120
IEEE/CS Member, student	$160	$80	$120	$80
Nonmember, student	$200	$100	$150	$120

Late Preregistration Rates (after September 12, 2021)

Late Preregistration Fees	Full ITC Conference	One Day 2 Tutorials	All-Access Tutorial Pass	One Workshop
IEEE/CS Member, non-author	$200	$120	$180	$120
Nonmember, non-author	$250	$150	$225	$150
IEEE/CS Member, author	$400	$120	$180	$120
Nonmember, author	$500	$150	$225	$150
IEEE/CS Member, student	$160	$120	$180	$120
Nonmember, student	$200	$150	$225	$150

Refunds

All refund/cancellation requests must be received in writing to registration+ITC@computer.org by **30 September 2021, 11:59 PM Eastern Time.** There will be an administrative fee of **US$10** for cancelled registrations

1. The ITC Final Program was generated with Adobe Acrobat 8.2.6 on 11 October 2021

2. The program will be updated periodically as new material is available - check back often.

3. Navigate using the tabs and links at the top of each page.

4. Use underlined links in the At-a-Glance to find specific items.

5. For more information contact:

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