INTERNATIONAL TEST CONFERENCE
OCTOBER 10-15, 2021
VIRTUAL CONFERENCE
CALL FOR PAPERS

The International Test Conference (ITC) is the world's premier venue dedicated to the electronic test of devices, boards and systems—covering the complete cycle from design verification, design-for-test, design-for-manufacturing, silicon debug, manufacturing test, system test, diagnosis, reliability and failure analysis, and back to process and design improvement. ITC will be virtual this year.

Emerging technologies such as optical, biomedical, and quantum devices will require new test solutions. Artificial Intelligence (AI) and the need for trustworthy devices are providing both new challenges and new opportunities for off-chip and on-chip test. At the same time, more stringent quality requirements, especially in automotive applications, are requiring more efficient test, debug, monitoring, and repair techniques that can transfer to the field.

Authors are invited to submit original, unpublished papers describing recent work in the field of test and design. Of particular interest are works dedicated to the topics listed on the right and/or works focused on special tracks such as Automotive, AI, or Security. Authors are also invited to submit practical, industry best practices papers. A special **industrial paper track** that focuses on case studies and practical examples is also available. Such papers will be limited to 5 pages in the final proceedings. The primary author on these submissions must be from industry. Industrial authors who want a longer paper in the proceedings should submit to one of the regular tracks. Submissions simultaneously under review or accepted by another conference, symposium or journal, will be summarily rejected.

Submissions must include:

- Title of paper.
- Name, affiliation, e-mail address of each author.
- The corresponding author(s). ITC will communicate with the corresponding author(s).
- One or two topic(s) from the topic list, or a description of your topic.
- An electronic copy of a complete paper of six pages (with a maximum of 10) for regular papers. Regular submissions of less than four pages are rarely accepted. Industrial track papers are limited to a maximum of five pages.
- An abstract of 100 words or less to be entered online.

ITC maintains a competitive selection process for technical papers. Submissions must clearly describe the status of the reported work, its contribution, novelty and/or significance. Supporting data, results (priority is often given to papers with results from real designs) and conclusions, and references to prior work must also be included. ITC does not accept submissions that do not meet the specified criteria.

Paper title/abstract due:	**April 23 2021**
Paper final PDF due:	**May 7, 2021**
Author notification:	**July 15, 2021**
Final manuscript due:	**Aug 20, 2021**

Authors are also invited to submit a **single-page** poster proposal. Posters are a useful way of presenting late-breaking results, getting feedback on an innovative method, or participating without having to write a full paper. Acceptance as a poster does not preclude submission of a more complete work as an ITC paper in 2022. Additional information on poster submissions will be provided on the ITC web page.

Poster submission deadline:	**June 7, 2021**
Author notification:	**July 29, 2021**

Test Week tutorial and workshop proposals are also welcomed. Deadlines and other information about proposals can be obtained from TTTC at: http://tab.computer.org/tttc

For detailed information about the submission process, requirements and deadlines, the selection process and any other questions regarding the program itself or contact information, please consult the ITC web site at http://www.itctestweek.org.

ITC invites submissions on the latest advances in test, validation and diagnosis of ICs, boards and systems.

Topics of interest include
(but not limited to)**:**

3D/2.5D Test
Adaptive Test in Practice
Artificial Intelligence (AI)/Machine Learning in Test
ATE/Probe Card Design
Automotive Test
Advances in Boundary Scan
Bring-Up
Data Driven Methods
Data Exchange and Infrastructure
Defect-oriented Testing
DFM and Test
Diagnosis
Economics of Test
End-to-End Data Analysis
End-to-End System Security
Embedded BIST and DFT
Emerging Defect Mechanisms
Field Monitoring, Test, & Debug
Hardware Security and Trust
IoT Testing
Jitter, High-Speed I/O and RF Test
Known-Good-Die testing
Memory Test and Repair
MEMS Testing
Mixed-Signal and Analog Test
New Technologies and Test
On-Chip Test Compression
Online Test
Pre-Silicon Verification
Post- Silicon Validation
Power Issues in Test
Protocol-aware Test
Quantum Device Testing
Reliability and Resilience
Scan Based Test
SoC/SiP/NoC Test
Silicon Debug
Simulation and Emulation
System Test (Applications)
System Test (Hardware/Software)
Test-to-Design Feedback
Test Escape Analysis
Test Flow Optimizations
Test Generation and Validation
Test Resource Partitioning
Test Standards
Test Time Analysis and Reduction
Testing High Speed Optics/Photonics
Timing Test
Yield Analysis and Optimization

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