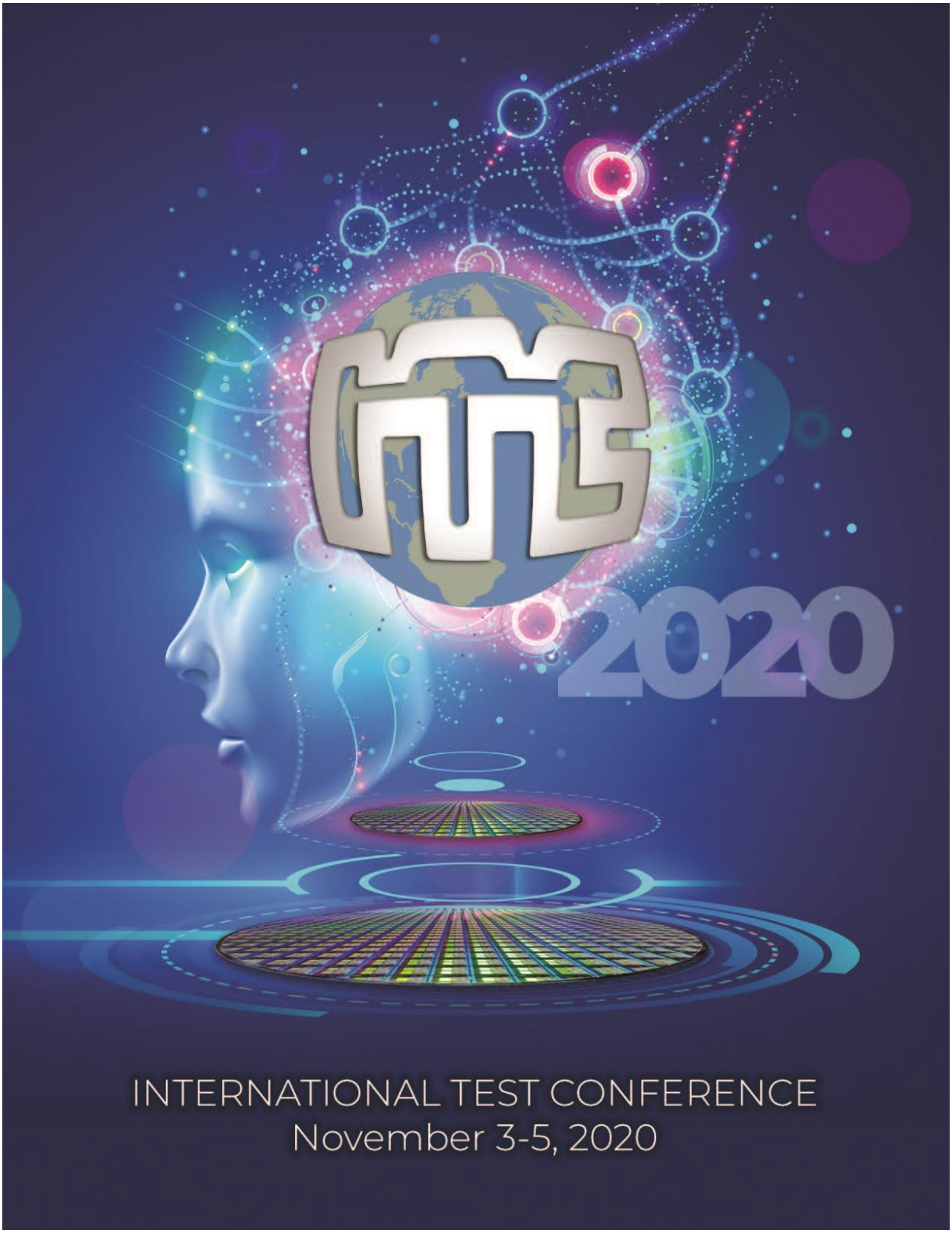
ITC
2020
INTERNATIONAL TEST CONFERENCE
November 3-5, 2020

ITC Welcome Message

It is our privilege to welcome you to the 51st International Test Conference (ITC) sponsored by IEEE and the IEEE Philadelphia Section. ITC is the world's premier conference dedicated to electronics test. Our volunteer committees worked very hard to provide to you an exciting event with a balance of the latest research and practical techniques related to electronics test. In this exceptional pandemic year, taking the safety of all participants into consideration, we have moved to a fully online conference with shorter days to maximize the opportunity to attend from home or office without any travel being required.

As we start the second half century of ITC, the program will look at a variety of traditional and emerging areas of test. Analog, ATE, and DFT-based papers form an important part of the program. This year we also had a record number of submissions for testing with and for AI. Specifically, the use of AI algorithms and techniques to improve test, debug, and diagnosis was well-represented, while other AI-focused submissions concentrated on AI hardware. Secure and Trusted Electronics will also be an important focus of multiple sessions on Wednesday, while Automotive test will once again consist of its own track on Thursday—leading naturally into the leading into the Automotive Test Workshop which immediately follows the conference, also in online format. Each day of the conference will begin with a memorable keynote address, and later sessions will include panels, posters, and a chance to visit ITC exhibits.

We have selected three papers based on reviewers' scores to be Distinguished Papers. These outstanding papers will be identified in the program. We are also continuing the inclusion of **Industrial Practice (IP) papers** in the conference to provide an opportunity to showcase important case studies and other approaches proven in an industrial environment. We are also introducing a new category of papers—**Short papers** that will be included in the proceedings and conference with a reduced length compared to regular papers. **Short Papers** and **IP Papers** will be clearly marked as such. in both the conference and the formal proceedings of ITC.

ITC is also continuing its expanded presence! For the fourth year, in 2020 there are ITC-Asia and ITC-India conferences in Taiwan and Bangalore respectively.

The conference is organized in a way to provide you various methods to learn and discuss topics related to electronics test. Our keynote speakers are well known industry leaders and academic researchers that provide exciting insights. Papers in the technical program were selected through a rigorous review process. Regular technical papers will be presented in 20-minute time slots, with a few minutes for questions at the end of each paper. Short Papers and IP papers will each have 15-minute time slots (including questions) allocated during the conference for presentation of the work.

The traditional exhibition floor has been replaced with online exhibition "booths". Solutions providers will be available for discussion and learning about their offerings and one-on-one meetings will be easy to arrange. A corporate forum is held online and merged into the program, where exhibiting companies present about their products. This year we have one poster session held in a dedicated time slot with the ability to interact directly with the authors. Posters provide a very comfortable and informal environment to discuss details.

We recognize that networking is extremely valuable to our attendees. The online platform makes it easy to connect with colleagues and other specialists via chat rooms.

On behalf of the 2020 International Test Conference steering committee, program committee and all the dedicated volunteers who are key to making the program complete, we welcome you to this year's exciting technical program and exhibits.

Peter Maxwell
General Chair

Jennifer Dworak
Program Chair

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	Sunday	Monday	Tuesday	Wednesday	Thursday	Friday
12 Half-Day TTTC Tutorials A great way to prepare for the ITC Technical program	●	●				
Four Panels			●		●	
Plenary Session and Keynotes			●	●	●	
64 Technical Presentations		●	●	●	●	
Three Tracks: AI, Security and Automotive			●	●	●	
World-Class Exhibits Virtual Exhibit Booths			●	●	●	
Corporate Forum The latest technical innovations from our exhibitors and corporate supporters			●	●		
Posters				●		
Two-Day Workshops Two to choose from					●	●
Virtual Meeting Rooms	●	●	●	●	●	●

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SUNDAY, NOVEMBER 1 – HALF-DAY TUTORIALS			
8:30 a.m. – 12:00 p.m.	Tutorial 1 Test Challenges and Solutions for Non-Volatile Memory Design	Tutorial 2 Defect-Based Testing: Selecting Right Fault Models, Creating New Ones	Tutorial 3 AI Chip Technologies and DFT Methodologies
1:00 p.m. – 4:30 p.m.	Tutorial 4 Machine Learning in Data Analytics	Tutorial 5 Mixed-Signal DFT and BIST: Trends, Principles and Solutions	Tutorial 6 Testing of TSV-based 2.5D- and 3D-Stacked ICs

MONDAY, NOVEMBER 2 – HALF-DAY TUTORIALS			
8:30 a.m. – 12:00 p.m.	Tutorial 7 Advances in FINFET Memory Test & Repair for Complex SOCs	Tutorial 8 Applications of Machine Learning in Semiconductor Manufacturing and Test	Tutorial 9 Improving ATPG Test Quality of Digital ICs
1:00 p.m. – 4:30 p.m.	Tutorial 10 Automotive Safety, Reliability and Test Solutions	Tutorial 11 Advances in Defect-Oriented Testing	Tutorial 12 From Test to Post-Silicon Validation: Concepts and Recent Trends

TUESDAY, NOVEMBER 3 – TECHNICAL SESSIONS				
10:00 a.m. – 11:00 a.m.	Plenary – Opening Session Keynote: Applying Digital Transformation Technologies to Semiconductor Product Development *Ritu Favre*, NI			
11:00 a.m. – 5:30 p.m.	Exhibits			
11:00 a.m. – 11:30 a.m.	Social/Exhibits			
11:30 a.m. – 12:30 p.m.	Session 1A Learning for Failure Analysis and Prediction	Session 1B Novel Test Pattern Generation	Session 1C Test and Mitigation with Analog and RF	Session 1D Interconnect Testing and Test Access (IP Papers)
12:30 p.m. – 1:30 p.m.	Social/Exhibits			
1:00 p.m. – 2:00p.m.	Session 2A Enhancing Yield and Diagnosis	Session 2B Special Session on Chiplet	Session 2C Sensing and Modeling for Analog and RF	Session 2D Microprocessor and Memory Test (IP Papers)
2:30 p.m. – 3:30 p.m.	Diamond Supporter Presentation			
3:30 p.m. – 5:00 p.m.	Panel 1		Panel 2	

All Times are Eastern Standard Time

WEDNESDAY, NOVEMBER 4 – TECHNICAL SESSIONS				
10:00 a.m.–11:00 a.m.	Plenary Session Keynote: Reverse Engineering Visual Intelligence, *James J. DiCarlo, MIT*			
11:00 a.m. – 5:30 p.m.	Exhibits			
11:30 a.m.–12:30 p.m.	Session 3A 2020 ITC Paper Highlights	Session 3B Machine Learning Hardware and Applications	Session 3C Ensuring Secure and Trustworthy Circuitry	Session 3D TTTC PhD Competition Asia/Europe
12:30 p.m.–1:00 p.m.	Social/Exhibits			
1:00 p.m.–2:00p.m.	Session 4A Machine Learning for Reliable Operation	Session 4B IEEE 1687 and Reconfigurable Scan	Session 4C Security, Safety & Emerging Devices (Short Papers)	Session 4D TTTC PhD Competition Latin America/US
2:00 p.m.–2:30p.m.	Break before Exhibit Presentations			
2:30 p.m.–3:30 p.m.	Exhibit Presentations			
3:30 p.m.–5:00 p.m.	Poster Session			

THURSDAY, NOVEMBER 5– TECHNICAL SESSIONS				
10:00 a.m – 11:00 a.m.	Plenary Session Keynote: 50 Years of ITC! Now What? *Rob Aitken, Arm Fellow, Arm*			
11:00 a.m – 11:30 a.m	Social/Exhibits			
11:00 a.m. – 5:30 p.m.	Exhibits			
11:30 a.m.–12:30 p.m.	Session 5A Best Practices in Safety (Automotive Track)	Session 5B Diagnosis & Repair	Session 5C Fault Modeling and DFT (Short Papers)	Session 5D ITC Asia 2020 Top 3 Papers
12:30 p.m. – 1:00 p.m.	Social/Exhibits			
1:00 p.m.–2:00 p.m.	Session 6A Quality, Test & Analysis (Automotive Track)	Session 6B DFT for Complex Systems	Session 6C Embedded Tutorials (Quantum Computing, Machine Learning)	Session 6D Learning & Data Analysis (IP Papers)
2:00 p.m.– 2:30 p.m.	Break before Exhibit Presentations			
2:30 p.m.– 3:30 p.m.	Exhibitor Presentations			
3:30 p.m. – 5:00 p.m.	Panel 3 Automotive Track Panel		Panel 4	

THURSDAY, NOVEMBER 5 – WORKSHOPS		
4:00 p.m. – 4:30 p.m.	Opening Address	
4:30 p.m. – 6:30 p.m.	Automotive Reliability and Test	3D & Chiplet Test Workshop

FRIDAY, NOVEMBER 6 – WORKSHOPS		
8:00 a.m. – 4:00 p.m.	Automotive Reliability and Test	3D & Chiplet Test Workshop

Security Track **Automotive Track** **AI Track**

All times are Eastern Standard Time

TTTC TEST TECHNOLOGY EDUCATION PROGRAM (TTEP) 2020

The Tutorials & Education Group of the IEEE Computer Society Test Technology Technical Council (TTTC) organizes a comprehensive set of Test Technology Tutorials to be held in conjunction with several TTTC-sponsored technical meetings worldwide. The mission of the Test Technology Educational Program (TTEP) is to serve test and design professionals by offering fundamental education and expert knowledge in state-of-the-art test technology topics. TTEP offers tutorial participants the opportunity to earn official certification from IEEE Computer Society TTTC. Each half-day tutorial corresponds to two TTEP units. Upon completion of 16 TTEP units, official recognition in the form of an IEEE TTTC Test Technology Certificate will be presented to the participant. For further information regarding TTEP, please visit http://ttep.tttc-events.org/ttep/index.html

At ITC 2020, TTTC/TTEP is pleased to present 12 **half-day tutorials** on topics of current interest to test professionals and researchers. All tutorials qualify for credit towards IEEE TTTC certification under the TTEP program. Six tutorials are held on Sunday, November 1. Six tutorials will be held on Monday, November 2.
The **one-day** tutorial registration fee is for two tutorials—a morning tutorial and afternoon tutorial, both on the same day, e.g., Tutorial 1 and Tutorial 4 on Sunday. You may register for up to four tutorials (two consecutive tutorials on Sunday and two consecutive tutorials on Monday).
The **all-access pass** tutorial registration provides in-and-out access to all twelve tutorials over both days.
(see registration page or http://www.itctestweek.org for further information).

Sunday 8:30 a.m. – 12:00 p.m. EST

TUTORIAL 1
Test Challenges and Solutions for Non-Volatile Memory Design

Presenter: S. Ghosh

At the end of Silicon roadmap, several emerging non-volatile memory (NVM) technologies have surfaced. Due to plentitude of features e.g., non-volatility, capability to create new computation paradigms, scalability and low power, these NVMs have created substantial excitement in the design community. This tutorial will uncover the test challenges associated with some of these promising technologies e.g., Spin-Transfer Torque RAM and Resistive RAM that can be harmful for the yield. This is specifically true in high-volume manufacturing of large capacity NVM arrays. Role of test in assuring high degree of resiliency and memory integrity will also be discussed.

TUTORIAL 2
Defect-Based Testing: Selecting Right Fault Models, Creating New Ones

Presenters: R. Parekhji, W. Pradeep

Test generation has used the simplifying premise of approximate fault models to model real-life defects in silicon. This approximation has been the basis for the success of ATPG (automatic test pattern generation) tools which are ubiquitously used for today's designs. This tutorial provides an in-depth understanding of the evolution and choice of fault models as defects become increasingly parametric, (i.e. granular as against gross), for today's technologies, and how matching ATPG capabilities have been developed to catch these defects, while still keeping the test application time affordably low. The choice of selecting from an existing set of large generic fault models vs creating new defect specific fault models will be explained, together with supporting silicon fall-out results. While these methods are well developed for digital circuits, they are evolving for analog circuits. The tutorial will explain
how defect-based fault models are being applied to today's analog circuits and the resulting challenges therefrom. Capabilities built into EDA tools will also be presented.

TUTORIAL 3
AI Chip Technologies and DFT Methodologies

Presenters: Y. Huang, R. Singhal, L. Harrison

Hardware acceleration for Artificial Intelligence (AI) is now a very competitive and rapidly evolving market. In this tutorial, we will start by covering the basics of deep learning. We will proceed to give an overview of the new and exciting field of using AI chips to accelerate deep learning computations. Next, we will summarize the features of the AI chips from design-for-test (DFT) perspective and introduce the DFT technologies that can help testing AI chips and speeding up time-to-market. Finally, we will present a few case studies on how DFT is implemented on the real AI chips.

Sunday 1:00 p.m. – 4:30 p.m. EST

TUTORIAL 4
Machine Learning in Data Analytics

Presenter: L-C. Wang, Chuanhe (Jay) Shan

Applying "machine learning" (ML) in data analytics has received growing interests in recent years. Analysis of "data" originated from design and test processes has been a common practice in the semiconductor industry for decades, well before the modern ML became a hot topic. What are the potential added values brought by the modern ML to the existing data analytics practices in design and test? The first part of the tutorial provides a review of the basic principles for applying ML in selected applications and highlights gaps for achieving a deployable ML solution. The second part introduces the idea of Intelligent Engineering Assistant (IEA), designed to enable ML to be applied in a real-world application. Key technologies for implementing an IEA agent will be discussed. In principle, an IEA agent is an AI software system incorporating human perception in its analytics. Results based on actual industrial settings will be presented and discussed.

TUTORIAL 5
Mixed-Signal DFT and BIST: Trends, Principles and Solutions

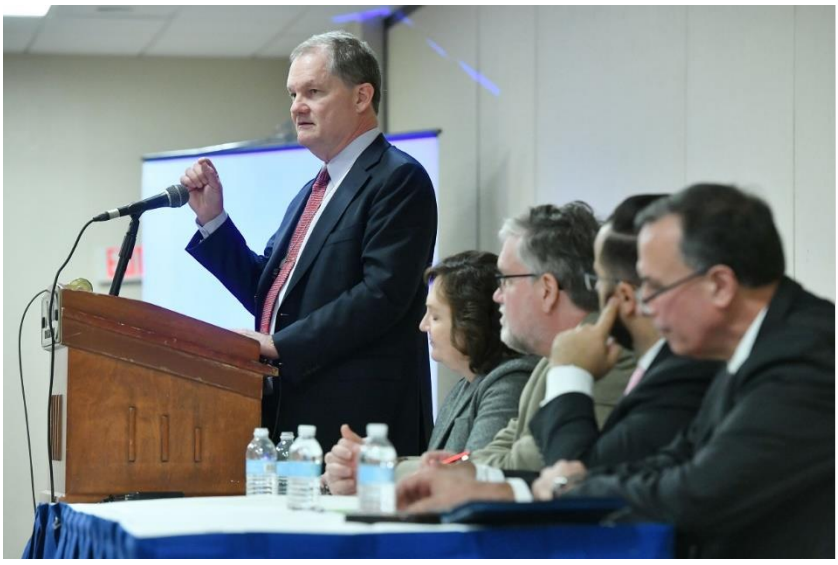
Presenter S. Sunter

This tutorial explores systematic analog design for test and analog fault simulation, especially for automotive ICs. We review trends in ad hoc DfT, fault simulation, IEEE 1149.1/4/6/7/8/10 (briefly), 1687, and ISO26262, then BIST for ADC/DAC, PLL, SerDes/DDR, and random analog. Essential principles of practical analog BIST are presented, then practical DfT techniques, from quicker analog defect simulation, to over/under sampling methods that improve range, resolution, and reusability. We conclude with a discussion of the Analog Defect Coverage and Test Access standards (P1687.2, P2427), and measurement of ISO 26262 metrics.

TUTORIAL 6
Testing of TSV-based 2.5D- and 3D-Stacked ICs

Presenter: E. J. Marinissen

3D-stacked ICs are moving from technology hype to real products. This timely tutorial first presents the fundamentals of 3D fabrication processes, defects, and fault modeling. Subsequently, we address the test challenges associated with 2.5D-/3D-stacked ICs, along with tried and tested solutions. Most 3D-test challenges pertain to (1) probe test access from test equipment to the dies, (2) 3D-DfT test access architectures across the stack (with special attention for the recently released standard IEEE Std 1838™-2019), and (3) test flow optimization to contain the overall stack cost. The tutorial presents data from various 3D test chips and early products.



Monday 8:30 a.m. – 12:00 p.m.

TUTORIAL 7
Advances in FINFET Memory Test & Repair for Complex SOCs

Presenter: Y. Zorian

Recent growth in artificial intelligence and large content delivery applications have led to an explosion in the utilization of memories, including on-chip embedded memories and off-chip high-bandwidth memories. This tutorial will start with the trends and challenges of growing memory utilization in SOCs and then discuss how to meet test and repair requirements for today's defects in advanced technology nodes, down to 4nm. These include FinFET, aging, reliability, process variation failures, which occur in manufacturing flow and during semiconductor lifecycle. The tutorial will cover the BIST and Repair solutions to address debug, diagnosis, yield optimization and data retention. Given the tens of thousands of embedded memory instances in today's SOCs, it will also cover the memory BIST architectural trade-offs, power management constraints, timing implications, test scheduling optimization, and area minimization options.

TUTORIAL 8
Applications of Machine Learning in Semiconductor Manufacturing and Test

Presenters: H. Stratigopolos, Y. Makris

Throughout the lifetime of an integrated circuit, a wealth of data is collected for ensuring its reliable operation. Ranging from design-time simulations to process characterization monitors, and from high-volume specification tests to diagnostic measurements on customer returns, the information inherent in this data is invaluable. Mining this information using machine learning methods has seen intense interest and numerous breakthroughs during the last decade. This tutorial seeks to elucidate the utility of machine learning in semiconductor manufacturing and test. Relevant concepts from machine learning will be introduced, agglomerated with current practice, and showcased using industrial data. Recommendations for practitioners will also be given.

TUTORIAL 9
Improving ATPG Test Quality of Digital ICs

Presenters: E. J. Marinissen, A. Singh

This tutorial presents motivation, algorithmic concepts, and industrial results obtained in the quest to improve ATPG test quality for digital ICs. First, we review traditional scan stuck-at and timing-based tests, with a focus on which defects might escape detection. Next, we discuss N-Detect and Embedded Multi-Detect. As intracell defects are typically not on the radar screen of conventional ATPG tools, test quality is improved by explicitly going after these defects. In this context, we discuss Gate/Cell Exhaustive Test, Cell-Aware Test, and its recent Timing-Aware variant aimed at small-delay defects. The effectiveness of these new test methods is discussed based on experimental and volume-production results obtained for CMOS cell libraries from 90nm down to 14nm FinFET, and even 3nm FinFET.

Monday 1:00 p.m. – 4:30 p.m. EST

TUTORIAL 10
Automotive Safety, Reliability and Test Solutions

Presenters: R. Mariani, Y. Zorian

Given today's fast-growing automotive semiconductor industry, this tutorial will discuss the implications of automotive quality, functional safety, and reliability on all aspects of automotive SOC lifecycle, while accelerating time to market for these semiconductor ICs. The automotive SOC lifecycle stages will include design, silicon bring-up, volume production, and particularly in-system operation. Today's automotive safety critical chips need multiple in-system modes, such as power-on and power-off self-test and repair (key-on/key-off), periodic in-field self-test during mission mode, advanced error correction solutions, etc. This tutorial will analyze these specific in-system test modes and the discuss the benefits of using ISO 26262 including its second edition, and several newer standardization efforts, in order to ensure that standardized functional safety requirements are met.

TUTORIAL 11
Advances in Defect-Oriented Testing

Presenter: A. Singh

Recent experience indicates that traditional logic level stuck-at and TDF scan test methodologies can miss significant defectivity that is better captured by new defect-oriented fault models that explicitly target potential defect locations based on the layout. In this tutorial, we present the latest in defect-oriented test methodology, from its initial focus on cell internal defects, to the most recent advances that comprehensively cover inter-cell defects, as well as bridges and opens in the interconnect network. Timing aware cell aware tests also minimize timing slack for small delay defect detection. Test effectiveness is discussed based on volume data from industrial studies.

TUTORIAL 12
From Test to Post-Silicon Validation: Concepts and Recent Trends

Presenters A. Sinha, S. Ray

The tutorial provides a broad overview of post-silicon bring-up, debug, and diagnosis, and discusses fundamental concepts and current practices. It introduces the spectrum of validation activities, e.g., functionality, software compatibility, electrical characteristics, speed path, etc. Activities involved in validation planning along the system life cycle and various conflicts and trade-offs are discussed. The trade-offs span a spectrum of topics, including security, power management, and physical design. The tutorial will describe approaches to repurpose Design-for-Test (DFT) infrastructure for post-silicon validation, and the collaboration areas between validation and test. Instrumentation, control, and observability technologies including tracing and triggering, scan and array dumping, and off-chip transport will be addressed. The focus of the tutorial is on industrial adoption and practice.

ITC Exhibitors*

Advantest

Defacto Technologies

ELES Semiconductor Equipment Spa

GOEPEL Electronics LLC

INNO GLOBAL

Mentor, A Siemens Business

Roos Instruments

STAr Technologies

Synopsys, Inc.

TTTC

** As of publication date*

Corporate Forum

The Corporate Forum track provides an opportunity for ITC exhibitors and supporters to present information on their latest products and services. More details will appear in subsequent releases of the Advance Program.

Tuesday 10:00 a.m. – 11:00 a.m.

Opening Remarks
Peter Maxwell, *ITC 2020 General Chair*

ITC 2020 Program Introduction
Jennifer Dworak, *ITC 2020 Program Chair*

ITC 2019 Paper Awards Presentation
Peter Maxwell, *ITC 2017 Program Chair*

TTTC Awards Presentation
Yervant Zorian

Keynote Address

Applying Digital Transformation Technologies to Semiconductor Product Development

Ritu Favre *Senior Vice President and General Manager of Semiconductor Busines, NI*

At first glance, you might think that digital transformation applies only to IT organizations, e-commerce systems, or your personal strategy to store family photos in the cloud. However, many of the same technologies that improve our consumer experiences are are fundamentally shaping how semiconductor organizations design, test, and manufacture semiconductor products. In this presentation, we'll share some of the latest trends and technologies that best-in-class semiconductor companies are using to accelerate and improve product designs. More specifically, we'll share practical examples of how companies are utilizing technologies ranging from the remote automation to the cloud to artificial intelligence to transform modern engineering labs and enterprises.

About the speaker As senior vice president and general manager of the semiconductor business, Ritu Favre is responsible for driving business growth and defining the products, services, and capabilities required to meet the unique needs of NI customers in the market.

Favre is a seasoned high-tech industry leader with experience across general management and executive leadership roles in the RF and semiconductor industries. Most recently, she served as the chief executive officer of NEXT Biometrics and was on the Cohu Board of Directors. Prior to her role at NEXT, she helped build profitable businesses while holding senior management positions with market leaders such as Motorola, Freescale Semiconductor, and Synaptics.

Favre is a member of the Global Semiconductor Association's Women's Leadership Council, which is aimed at inspiring and sponsoring the next generation of female leaders in the semiconductor industry. She received both her bachelor's and master's degrees in electrical engineering from Arizona State University.

10:00 a.m. – 11:00 a.m.

Reverse Engineering Visual Intelligence

James J. DiCarlo *Peter deFlorenz Professor of Neuroscience, Massachusetts Institute of Technology*

The brain and cognitive sciences are hard at work on a great scientific quest — to reverse engineer the human mind and its intelligent behavior. Yet these field are still in their infancy. Not surprisingly, forward engineering approaches that aim to emulate human intelligence (HI) in artificial systems (AI) are also still in their infancy. Yet the intelligence and cognitive flexibility apparent in human behavior are an existence proof that machines can be constructed to emulate and work alongside the human mind.

In this session, I will focus on one aspect of human intelligence — visual object categorization and detection — and I will tell the story of how work in brain science, cognitive science and computer science converged to create deep neural networks that can support such tasks. These networks not only reach human performance for many images, but their internal workings are modeled after— and largely explain and predict — the internal workings of the primate visual system. Yet, the primate visual system (HI) still outperforms current generation artificial deep neural networks (AI), and I will show some new clues that the brain and cognitive sciences can offer.

These recent successes and related work suggest that the brain and cognitive sciences community is poised to embrace a powerful new research paradigm. More broadly, our species is the beginning of its most important science quest — the quest to understand human intelligence — and I hope to motivate others to engage that frontier alongside us.

About the speaker James DiCarlo is a Professor of Neuroscience, and Head of the Department of Brain and Cognitive Sciences at the Massachusetts Institute of Technology. His research goal is to reverse engineer the brain mechanisms that underlie human visual intelligence. He and his collaborators have revealed how population image transformations carried out by a deep stack of neocortical processing stages -- called the primate ventral visual stream -- are effortlessly able to extract object identity from visual images. His team uses a combination of large-scale neurophysiology, brain imaging, direct neural perturbation methods, and machine learning methods to build and test artificial neural network models of the ventral visual stream and its support of cognition and behavior. Such an engineering-based understanding is likely to lead to new artificial vision and artificial intelligence approaches, new brain-machine interfaces to restore or augment lost senses, and a new foundation to ameliorate disorders of the mind.

10:00 a.m. – 11:00 a.m.

50 Years of ITC! Now What?

Rob Aitken *ARM Fellow and Technology Lead, ARM Research, ARM*

Last year we collectively celebrated the 50th International Test Conference. After 50 years it's tempting to say that everything's been done, or conversely to look ahead to a glorious but only vaguely specified future. As test professionals, we know that better analysis of existing data can help us to identify and respond to future challenges. Today's challenges include a slowing of Moore's Law coupled with an ever-increasing appetite for data and analytics. Security and privacy concerns abound. Machine learning gives fast answers but few reasons. New technologies are emerging and bringing new test challenges with them. This talk takes stock of where we are and how we got here, and then focuses on where we might go next and why.

About the speaker Rob Aitken is an ARM Fellow and technology lead for ARM Research. He is responsible for technology direction of ARM research, including identifying disruptive technologies, monitoring the global technology landscape, and coordinating research efforts within and outside of ARM. He has worked on test and related topics for 35 years, and is a former general chair and program chair of ITC. He has published over 100 technical papers, on a wide range of topics. He holds over 40 US patents. Dr. Aitken joined ARM as part of its acquisition of Artisan Components in 2004. Prior to Artisan, he worked at Agilent and HP. He is an IEEE Fellow and holds a Ph.D. from McGill University in Canada.
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11:30 a.m. – 12:30 p.m. EST

SESSION 1A
Learning for Failure Analysis and Prediction
(Chair)

1A.1 LAIDAR: Learning for Accurate and Ideal Diagnostic Resolution
Q. Huang, C. Fang, S. Blanton, Carnegie Mellon University

1A.2 Unsupervised Root-Cause Analysis for Integrated Systems
R. Pan, X. Li, Duke University; *Z. Zhang, X. Gu*, Futurewei Technogies; *K. Chakrabarty*, Department of Electrical and Computer Engineering, Duke University

1A.3 Unleashing the Power of Anomaly Data for Soft Failure Predictive Analytics
F. Su, P. Goteti, Intel Corp; *M. Zhang*, University of Michigan - Ann Arbor

SESSION 1B
Novel Test Pattern Generation

1B.1 qATG: Automatic Test Generation for Quantum Circuits
C-H. Wu, C-Y. Hsieh, J-M. Li, National Taiwan University

1B.2 Functional Test Sequences for inducing Voltage Droops in a Multi-Threaded Processor
V. Kalyanam, E. Mahurin, M. Spence, Qualcomm Technologies Inc; *J. Abraham*, University of Texas at Austin

1B.3 SAT-ATPG Generated Multi-Pattern Scan Tests for Cell Internal Defects: Coverage Analysis for Resistive Opens and Shorts
S. Pandey, Z. Liao, S. Nandi, A. Chatterjee, Georgia Institute of Technology; *S. Gupta*, Department of Electrical Engineering, University of Southern California; *A. Sinha, S. Natarajan*, Intel Corporation; *A. Singh*, Auburn University

SESSION 1C
Test and Mitigation with Analog and RF

1C.1 Fast EVM Tuning of MIMO Wireless Systems Using Collaborative Parallel Testing and Implicit Reward Driven Learning
S. Komarraju, A. Chatterjee, Georgia Institute of Technology

1C.2 Robust DfT Techniques for Built-in Fault Detection in Operational Amplifiers with High Coverage
M. Saikiran, M. Ganji, D. Chen, Iowa State University

1C.3 Proactive Supply Noise Mitigation with Low-Latency Minor Voltage Regulator and Lightweight Current Prediction
J. Chen, M. Hashimoto, Osaka University

SESSION 1D
Interconnect Testing & Test Access (IP Papers)

1D.1 IJTAG Through a Two-Pin Chip Interface
M. Baby, B. Buettner, P. Engelke, U. Pfannkuchen, Infineon Technologies AG; *R. Meier*, Mentor, A Siemens Business; *J. Gaudet*, Mentor, A Siemens Business; *J-F. Côté*, Mentor, A Siemens Business; *G. Danialy*, Mentor, A Siemens Business; *M. Keim, L. Schramm*, Mentor

1D.2 High Speed Serial Links Risk Assessment in Industrial Post-Silicon Validation Exploiting Machine Learning Techniques, *C. Sanchez-Martinez, P. Lopez-Meyer, E. Juarez-Hernandez, A. Desiga-Orenday, A. Viveros-Wacher*, Intel Corporation

1D.3 Cost-Effective Test Method that can Screen out Unexpected Failure in High Speed Serial Interface IPs
S-U. Ahn, B-K. Seo, H-W. Kim, Y-S. Shin, H-T. Kim, G-G. Oh, Y-D. Kim, Samsung Foundry (Samsung Electronics Co. Ltd)

1D.4 Fast Bring-Up of an AI SoC through IEEE 1687 Integrating Embedded TAPs and IEEE 1500 Interfaces
H. Ma, L. Lu, H. Qian, J. Han, Enflame Technology; *X. Wen*, Mentor, A Siemens Business; *F. Meng*, Mentor, A Siemens Business; *M. Keim*, Mentor; *W. Yang*, Mentor, a Siemens Company; *R. Singhal*, Mentor, A Siemens Business; *Y. Huang*, Mentor, A Siemens Business

1:00 p.m. – 2:00 p.m.

SESSION 2A
Enhancing Yield and Diagnosis

2A.1 Improved Chain Diagnosis Methodology with clock and control signal defect identification
N. L'Esperance, R. Redburn, IBM; *B. Nandakumar, A. Chhabra, S. Chillarige*, Cadence Design Systems; *A. Malik*, Cadence Design Systems (I) Pvt Ltd.

2A.2 Automating Design for Yield: Silicon Learning to Predictive Models and Design Optimization
S. Venkataaman, Intel Corporation

2A.3 High Defect-Density Yield Learning using Three-Dimensional Logic Test Chips
Z. Liu, R. Blanton, Carnegie Mellon University

SESSION 2B
Special Session on Chiplet
Yervant Zorian, Chair

SESSION 2C
Sensing and Modeling for Analog & RF

2C.1 Rapid PLL Monitoring by a Novel Min-Max Time-to-Digital Converter
W-H. Chen, National Tsing Hua University, Taiwan; *C-C. Hsu*, National Tsing Hua University, Taiwan; *S-Y. Huang*, National Tsing Hua University, Taiwan

2C.2 Modeling Accuracy of Wideband Power Amplifiers with Memory Effects via Measurements
W. Gao, Broadcom; *T. Jing*, Northwest University

2C.3 Design Optimization for N-port RF Network Analyzers under Noise and Gain Imperfections
M. Avci, S. Ozev, Arizona State University

SESSION 2D
Microprocessor & Memory Test (IP Papers)

2D.1 Test Challenges of Intel IA Cores
K-H. Tsai, Mentor, A Siemens Business; *K. Wee, U. Shpiro*, Intel; *J. Zawada*, Mentor, A Siemens Business; *X. Lin*, Mentor, A Siemens Business

2D.2 Novel Eye Diagram Estimation Technique to Assess Signal Integrity in High-Speed Memory Test
Y. Oh, D. Han, B. Go, S. Lee, W. Jeong, SK Hynix

2D.3 Memory Repair Logic Sharing Techniques and their Impact on Yield
B. Nadeau-Dostie, Mentor; *L. Romain*, Mentor, A Siemens Business

2D.4 MBIST Supported Reliable eMRAM Sensing
J. Yun, B. Nadeau-Dostie, M. Keim, L. Schramm, Mentor; *C. Dray, M. Boujamaa, K. Gelda*, ARM

11:30 a.m. – 12:30 p.m. Eastern Standard Time

SESSION 3A
2020 ITC Paper Highlights

3A.1 Learning A Wafer Feature with One Training Sample
Y. Zeng, University of California Santa Barbara; *L-C. Wang*, University of California Santa Barbara; *C. Shan*, IE3A, Inc.; *N. Sumikawa*, NXP

3A.2 Characterization, Modeling, and Test of Synthetic Anti-Ferromagnet Flip Defect in STT-MRAMs
L. Wu, M. Taouil, S. Hamdioui, Delft University of Technology; *S. Rao, E. Marinissen, G. Kar*, IMEC

3A.3 Industrial Application of IJTAG Standards to the Test of Big-A/little-d devices
H. von Staudt, M. Benhebibi, M. Laisne, Dialog Semiconductor; *J. Rearick*, Advanced Micro Devices

SESSION 3B
Machine Learning Hardware and Applications (Short Papers)

3B.1 Concurrent detection of failures in GPU control logic for reliable parallel computing
H. Itsuji, Center for Technology Innovation - Production Engineering, Research & Development Group; *T. Uezono*, Center for Technology Innovation - Production Engineering, Research & Development Group; *T. Toba*, Center for Technology Innovation - Production Engineering, Research & Development Group; *K. Ito*, Department of Information Systems Engineering, Osaka University; *M. Hashimoto*, Osaka University

3B.2 Functional Criticality Classification of Structural Faults in AI Accelerators
A. Chaudhuri, J. Talukdar, Duke University; *F. Su*, Intel Corp; *K. Chakrabarty*, Department of Electrical and Computer Engineering, Duke University

3B.3 Automated Assertion Generation from Natural Language Specifications
S. Frederiksen, J. Aromando, M. Hsiao, Virginia Tech

3B.4 Machine Intelligence for Efficient Test Pattern Generation
S. Roy, S. Millican, V. Agrawal, Auburn University

SESSION 3C
Ensuring Secure and Trustworthy Circuitry

3C.1 SPARTA: A Laser Probing Approach for Trojan Detection
A. Stern, D. Mehta, S. Tajik, F. Farahmandi, M. Tehranipoor, University of Florida

3C.2 A Weak Asynchronous RESet (ARES) PUF Using Start-up Characteristics of Null Conventional Logic Gates
S. Chowdhury, R. Acharya, W. Boullion, D. Forte, University of Florida; *M. Howard, A. Felder, J. Di*, University of Arkansas

3C.3 Schmitt Trigger-Based Key Provisioning for Locking Analog/RF~Integrated~Circuits
A. Sanabria-Borbón, N. Gummidipoondi Jayasankaran, J. Hu, J. Rajendran, E. Sánchez-Sinencio, Texas A&M University; *S. Lee*, SK Hynix

SESSION 3D
TTTC-PhD Competition (Asia/Europe)

3D.1 Digital Design Techniques for Dependable High-Performance Computing
S. Azimi, Politecnico di Torino

3D.2 Assuring Security and Reliability of Emerging Non-Volatile Memories
M. Khan, Penn. State Univ.

1:00 p.m. – 2:00 p.m.

SESSION 4A
Machine Learning for Reliable Operation

4A.1 FAT: Training Neural Networks for Reliable Inference Under Hardware Faults
U. Zahid, G. Gambardella, N. Fraser, M. Blott, K. Vissers, Xilinx

4A.2 Online Fault Detection in ReRAM-Based Computing Systems by Monitoring Dynamic Power Consumption
M. Liu, Duke University; *K. Chakrabarty*, Duke University

4A.3 Advanced Outlier Detection Using Unsupervised Learning for Screening Potential Customer Returns
H. Hu, University of California, Santa Barbara; *N. Nguyen, C. He*, NXP Semiconductors; *P. Li*, University of California, Santa Barbara

SESSION 4B
IEEE 1687 and Reconfigurable Scan

4B.1 Multi-Level Access Protection for Future IEEE P1687.1 IJTAG Networks
D. Brauchler III, J. Dworak, Southern Methodist University

4B.2 Modeling Novel Non-JTAG IEEE 1687-Like Architectures
M. Laisne, H. von Staudt, Dialog Semiconductor; *A. Crouch*, Amida Technology Solutions, Inc.; *M. Portolan*, Univ Grenoble Alpes; *M. Keim*, Mentor; *M. Abdalwahab*, NXP Semiconductors; *B. Van Treuren*, VT Enterprises Consulting Services; *J. Rearick*, Advanced Micro Devices

4B.3 Security Preserving Integration and Resynthesis of Reconfigurable Scan Networks
N. Lylina, A. Atteya, H-J. Wunderlich, University of Stuttgart; *C-H. Wang*, National Sun Yat-sen University

SESSION 4C
Security, Safety, & Emerging Devices (Short Papers)

4C.1 Avionics Simulation Environment
H. Sagirkayaz, Turkish Aerospace; *G. Durgun*, Simsoft Information Technologies

4C.2 Data-driven Fault Model Development for Superconducting Logic
M. Li, F. Wang, S. Gupta, University of Southern California

4C.3 BISTLock: Efficient IP Piracy Protection using BIST
S. Chen, Duke University; J. Jung, *P. Song*, IBM; *K. Chakrabarty*, Duke University; *G-J Nam*, IBM

4C.4 Cross PUF Attacks on Arbiter-PUFs through their Power Side-Channel
T. Kroeger, University of Maryland; *W. Cheng, S. Guilley, J-L Danger*, Institut Polytechnique de Paris; *N. Karimi*, University of Maryland

SESSION 4D
TTTC-PhD Competition (Latin America/US)

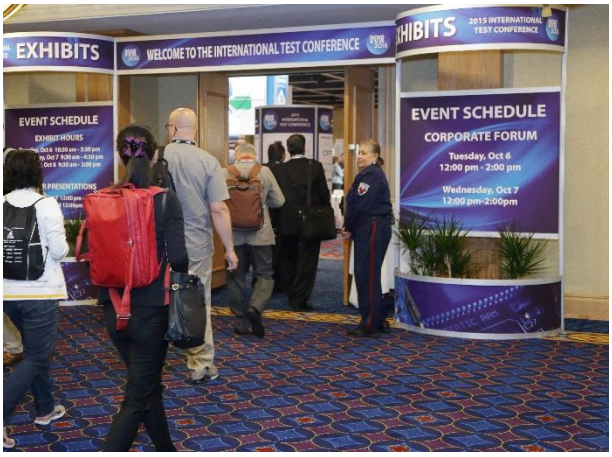
4D.1 Susceptibility Analysis of Logic Gates to Improve the Accuracy of Circuit Reliability Estimation
R. Schvittz, Federal University of Pelotas

4D.2 Hardware IP Protection Using Logic Encryption and Watermarking
R. Karmakar, S. Chattopadhyay, IIT Kharagpur

Security Track

AI Track

Automotive Track



11:30 a.m. – 12:30 p.m. EST

SESSION 5A
Best Practices in Safety (Automotive Track)
(Chair)

5A.1 Stress, Test, and Simulation of Analog IO Pads on Automotive ICs
C. He, S. Traynor, G. Bhagavatheeswaran, H. Sanchez, NXP Semiconductors

5A.2 Quick Analyses for Improving Reliability and Functional Safety of Mixed-Signal ICs
S. Sunter, M. Wolinski, Mentor, a Siemens Business; *A. Coyette, R. Vanhooren, W. Dobbelaere,* ON Semiconductor; *N. Xama, J. Gomez, G. Gielen,* KU Leuven

5A.3 On the Measurement of Safe Fault Failure Rates in High-Performance Compute Processors
R. Bramley, N. Saxena, P. Racunas, G. Duan, NVIDIA; *Y. Huang,* Mentor, A Siemens Business

SESSION 5B
Diagnosis & Repair
(Chair)

5B.1 A Learning-Based Cell-Aware Diagnosis Flow for Industrial Customer Returns
S. Mhamdi, P. Girard, A. Virazel, LIRMM, Univ. of Montpellier / CNRS; *A. Bosio,* Lyon Institute of Nanotechnology; *A. Ladhar,* STMicroelectronics

5B.2 Logic Fault Diagnosis of Hidden Delay Defects
S. Holst, Kyushu Institute of Technology; *M. Kampmann, A. Sprenger, J. Reimer, S. Hellebrand,* University of Paderborn; *H-J. Wunderlich,* University of Stuttgart; *X. Wen,* Mentor, A Siemens Business

5B.3 Fail Memory Configuration Set for RA Estimation
H. Lee, K. Cho, S. Kang, Dept. of Electrical and Electronic Engineering, Yonsei University; *W. Kang, S. Lee, W. Jeong,* SK Hynix

SESSION 5C
Fault Modeling and DFT (Short papers)
(Chair)

5C.1 A Unified Method of Designing Signature Analyzers for Digital and Mixed-Signal Circuits Testing
V. Geurkov, L. Kirischian, Ryerson University

5C.2 Selecting Close-to-Functional Path Delay Faults for Test Generation
I. Pomeranz, Purdue University

5C.3 Flip-flops Fanout Splitting in Scan Designs
M. Ladnushkin, Federal State Institution «Scientific Research Institute for System Analysis of the Russian Academy of Sciences»

SESSION 5D
ITC-Asia 2000 Top 3 Papers

1:00 p.m. – 2:00 p.m.

SESSION 6A
Quality Test & Analysis (Automotive Track)

6A.1 Wafer Level Stress: Enabling Zero Defect Quality for Automotive Microcontrollers without Package Burn-In
C. He, NXP Semiconductors; *Y. Yu,* NXP Semiconductor

6A.2 Concurrent Error Detection in Embedded Digital Control of Nonlinear Autonomous Systems Using Adaptive State Space Checks
M. Momtaz, C. Amarnath, A. Chatterjee, Georgia Institute of Technology

SESSION 6B
DFT for Complex Systems
(Chair)

6B.1 X-Tolerant Tunable Compactor for In-System Test
J. Tyszer, B. Wlodarczak, Poznan University of Technology; *Y. Liu, S. Milewski, G. Mrugalski, N. Mukherjee, J. Rajski,* Mentor, A Siemens Business

6B.2 Streaming Scan Network (SSN): An Efficient Packetized Data Network for Testing of Complex SoCs
J-F. Côté, M. Kassab, W. Janiszewski, R. Rodrigues; *R. Meier, B. Kaczmarek, P. Orlando*; *G. Eide, J. Rajski,* Mentor, A Siemens Business; *G. Colon-Bonet, Y. Yin, P. Pant, N. Mysore,* Intel Corporation

6B.3 At-speed DfT Architecture for Bundled-data Design
R. Aquino Guazzelli, L. Fesquet, TIMA Laboratory - Grenoble INP / UGA

SESSION 6C
Embedded Tutorials (Quantum Computing, Machine Learning)
(Chair)

6C.1 Introduction to Quantum Computation Reliability
M. Thornton, Southern Methodist University

SESSION 6D
Learning & Data Analysis (IP papers)
(Chair)

6D.1 Automated Socket Anomaly Detection through Deep Learning
N. Agrawal, Advantest America, Inc.; *C. Xanthopoulos,* The University of Texas at Dallas; *V. Thangamariappan,* Advantest America, Inc.; *J. Xiao,* ESSAI, Inc.; *C-W. Ho,* ESSAI, Inc.; *K. Schaub, I. Leventhal,* Advantest America, Inc.

6D.2 TestDNA-E: Wafer Defect Signature for Pattern Recognition by Ensemble Learning
L-Y. Chen, K-C. Cheng, A-A. Huang, N-Y. Tsai, L. Chou, C-S. Lee, NXP Semiconductors Taiwan Ltd.; *K-M. Li,* National Sun Yat-Sen University; *S-J. Wang,* National Chung Hsing University

6D.3 Machine Learning based Performance Prediction of Microcontrollers using Speed Monitors
R. Cantoro, R. Martone, G. Squillero, Politecnico di Torino; *M. Huch, T. Kilian,* Infineon Technology AG; *U. Schlichtmann,* Technical University of Munich *Kilian,* Infineon Technology AG; *U. Schlichtmann,* Technical University of Munich

6D.4 Using Volume Cell-aware Diagnosis Results to Improve Physical Failure Analysis Efficiency
H. Peng, M-Y. Hsia, M-T. Pang, I-Y. Chang, UMC; *J. Fan, H. Tang, M. Sharma,, W. Yang,* Mentor, a Siemens Company

Security Track

AI Track

Automotive Track

PO1 1687: A Deliberation
H. Bhagat, S. Pai, S. Smith, Marvell Semiconductors

PO2 At-speed Test with Hierarchical Wrapper Chain Techniques
R. Press, P. Girouard, T. Kobayashi, Mentor, a Siemens Business

PO3 Online Checkers to Detect Hardware Malware
S. R. Rajendran, Indian Institute of Technology Madras

PO4 A Simplified Method for Channel Loss Compensation and Bandwidth Extension to Accurately Characterize Digital and Serial Eye Patterns
T. Lyons, Teradyne

PO5 AI, 5G Autonomous Driving...What's Powering all this stuff? - Point of Load Regulator Trends, Test Challenges and Solutions
C. Carline, D. Marsh, Teradyne

PO6 Adaptive High Voltage Stress Methodology to Enable Automotive Quality in FinFet Technologies.
S. Traynor, C. He, Y. Yu, K. Klein, NXP

PO7 Test Power Reduction through Test Point Insertion.
Y. Sun, S. Millican, Auburn University

PO8 In-system Test Architecture for 7nm Automotive Designs
E. Im, J. Lee, B. Kim, Samsung; P. Chelmicki, L. Harrison, Mentor A Siemens Business

PO9 Utilizing both IEEE 1687 and IEEE 1500 Standards within a Single Design
. Neerkundar, R. Press, S. Shen, Mentor A Siemens Business

PO10 Design for Test with Data Driven Flow Automation
V. Neerkundar, Mentor A Siemens Business

PO11 Detecting Open Defects in Wires of On-Chip Power Grids by Measuring Resistances between Power Micro-Bumps
K. Hachiya, Teikyo Heisei University

PO12 Accelerated Analysis of Simulation Dumps through Parallelization on Multicore Architectures
A. Calabrese, P. Bernardi, S. Littardi, S. Quer, Politecnico di Torino

PO13 Testing and Modelling Composite Multiport Memories
R. Mehta, B. Nadeau-Dostie, V. Rajagopal, Mentor, A Siemens Business; S. Goyal, C. Swanson, K. Bajaj, Broadcom

PO14 Safe System-Handshake for Automotive Application
R. Mehta, N. Mukherjee, L. Harrison, Mentor, A Siemens Business; A. Priore, Arm

PO15 Switch-Mode Based Interposer developed to self-test an MCM without Known-Good-Dice
P. Shun, S. Wang, JTAG Technologies B.V.

PO16 A Holistic Approach In Testing Automotive Safety Products
S. Chonnad, V. Litovtchenko, Synopsys

Tuesday 3:30 p.m. – 5:00 p.m. EST

AUTOMOTIVE PANEL: TBA

PANEL 2: TBA

Thursday 3:30 p.m. – 5:00 p.m. EST

PANEL 3: TBA

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PANEL 4: TBA

IEEE Computer Society Test Technology Technical Council Workshops

Thursday and Friday

General Workshop Information

Two workshops are being held in parallel immediately following ITC 2020. They will each start with an opening address on Thursday afternoon, November 5, followed by a technical session. The remaining the technical sessions will be held on Friday, November 6. The technical scope of each workshop is described below.

Workshop Registration

All workshop participation requires registration. To register in advance for one of the workshops, do so online. Discount workshop registration rates apply until October 12, 2020. Workshop registration includes the opening address, technical sessions, and a digest of papers.

Digest of Papers

A digest of papers will be distributed only to attendees at the workshops as an informal proceedings.

Workshop Schedule

The three workshops will adhere to the same schedule:

Thursday, November 5		Friday, November 6	
Opening Address	4:00 p.m. – 4:30 p.m.	Technical Sessions	8:00 a.m. – 4:00 p.m.
Technical Session	4:30 p.m. – 6:30 p.m.		

Note: Workshop schedule is subject to change

Further Information

For more information on the workshops contact their organizers by e-mail or check the TTTC Web site http://ieee-tttc.org

ART 2020: IEEE Automotive Reliability and Test workshop 2020

The ART workshop focuses exclusively on test and reliability of automotive and mission-critical electronics, including design, manufacturing, burn-in, system-level integration and in-field test, diagnosis and repair solutions, as well as architectures and methods for reliable and safe operations under different environmental conditions. With increasing system complexity, security, stringent runtime requirements for functional safety, and cost constraints of a mass market, the reliable operation of electronics in safety-critical domains is still a major challenge. This edition of the ART Workshop offers a forum to present and discuss these challenges and emerging solutions among researchers and practitioners alike.

Functional safety and security in the automotive domain
Automotive standards and certification – ISO 26262
Approximate computing and artificial intelligence
Multilayer dependability evaluation
Verification and validation of automotive systems
Fault tolerance and self-checking circuits
Aging effects on automotive electronics
Resiliency by application
Dependability challenges of autonomous driving and e-mobility
Power-up, power-down and periodic test
System level test
Reuse of test infrastructure
Functional and structural test generation
High quality volume test- minimizing DPPM life-cycle test cost Minimization
Life cycle test cost minimization

General Chair: Yervant Zorian zorian@synopsys.com
Program Chair: Paolo Bernardi paolo.bernardi@polito.it

3DC-Test: 7th IEEE International Workshop on Testing Three-Dimensional, Chiplet-Based, and Stacked ICs

The 3DC-TEST Workshop focuses exclusively on test of and design-for-test for three-dimensional, chiplet-based, and stacked ICs (3D-SICs), including systems-in-package (SiP), package-on-package (PoP), 3D-SICs based on through-silicon vias (TSVs), micro-bumps, and/or interposers. While these stacked ICs offer many attractive advantages with respect to heterogeneous integration, small form-factor, high bandwidth and performance, and low power dissipation, there are many open issues with respect to testing such products. The 3DC-TEST Workshop offers a forum to present and discuss these challenges and (emerging) solutions among researchers and practitioners alike.

Topics include:

Defects due to wafer thinning
Defects in intra-stack interconnects
DfT architecture for 3D-SICs
EDA design-to-test flow for 3D-SICs
Failure analysis for 3D-SICs
Fault tolerant design for 3D-SICs
Handling and testing singulated stacks
Interposer testing
Known-good die / Stack testing
Open interface between chiplets
Standards for power/heat dissipation during test
Pre-, Mid- and Post-bond testing
Reliability of 3D-SICs
Stacking yield of dies, interconnects redundancy and repair
Standards for 3D testing incl. IEEE Std 1838™
Supply chain and logistics issues
System/Board test issues for 3D-SICs
Test cost modeling for 3D-SICs
Test flow optimization for 3D-SICs
Tester architecture incl. ATE and BIST
Thermal mechanical stress in 3D-SICs
Wafer probing and probe marks of 3D-SICs

General CoChairs: Erik Jan Marnissen, erik.jan.marinissen@imec.be
Yervant Zorian, mailto:yervant.zorian@synopsys.com

Program Chair: Bapi Vinnekota, bapi.vinnakota@ocproject.net

Registration Categories

Register Online

All Test Week activities require a registration badge for admittance. There are three registration periods with differing fees

- Early discount preregistration through October 12, 2020
- Non-discount preregistration October 13 to November 5, 2020.

▶ITC Full-Conference Registration Includes ITC technical paper and panel sessions, exhibits, and access to ITC 2020 papers, slides and presentations for one month after the conference. Registration does not include the tutorials on Sunday and Monday or the workshops on Thursday and Friday.

▶Tutorial Registration Tutorials are a half-day in length.
One-Day tutorial registration fee is for two tutorials—a morning tutorial and afternoon tutorial, both on the same day, e.g., Tutorial 1 and Tutorial 4 on Sunday. You may register for up to four tutorials (two consecutive on Sunday and two consecutive on Monday).
All-Access Pass tutorial registration provides in-and-out access to all twelve tutorials over both days.

All registrations include study material, breaks and lunches on the day(s) attended. Tutorial registration does not include the ITC technical program, ITC receptions, exhibits, exhibit hall lunches, ITC publications, ITC giveaways or the workshops on Thursday and Friday.

▶Workshop Registration Includes the items specified on page 23. Registration does not include the ITC technical program, exhibits, or the tutorials on Sunday and Monday.

▶Discount Rates Early registration rates apply only when you complete your registration by October 12, 2020, either online or with a paper form and payment postmarked or faxed by October 12, 2020. To receive IEEE member or student member reduced rates, you must include your member number, which will be verified.

Registration Fees

Early Preregistration Rates (on or before October 12, 2020)

Early Discount Preregistration Fees	Full Conference	One Day 2 Tutorials	All-Access Tutorial Pass	One Workshop
IEEE/CS Member, Non-author	$160	$80	$120	$80
Nonmember, non-author	$200	$120	$150	$120
IEEE/CS Member, author	$400	NA	NA	NA
Nonmember, author	$500	NA	NA	NA

Late Preregistration Rates (after October 12, 2020)

Late Preregistration Fees	Full ITC Conference	One Day 2 Tutorials	All-Access Tutorial Pass	One Workshop
IEEE/CS Member, non-author	$210	$120	$180	$120
Nonmember, non-author	$263	$150	$225	$150
IEEE/CS Member, author	$400	NA	NA	NA
Nonmember, author	$500	NA	NA	NA

Refunds

All refund/cancellation requests must be received in writing to registration+ITC@computer.org by **12 October, 2020, 11:59 PM Eastern Time.** There will be an administrative fee of **US$10** for cancelled registrations.

1. The ITC Advance Program release 0.2 was generated with Adobe Acrobat 8.2.6 on 27 September 2020

2. The program will be updated periodically as new material is available-check back often.

3. Navigate using the tabs and links at the top of each page.

4. Use underlined links in the At-a-Glance to find specific items.

5. For more information contact:

Subject	Contact	Email
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Fringe Technical Meetings	**IEEE Computer Society**	*ieeeitc@computer.org*
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Registration	**IEEE Computer Society**	*ieeeitc@computer.org*
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TTTC Tutorials	**Yervant Zorian**	*zorian@synopsys.com*
TTTC Workshops	**Yervant Zorian**	*zorian@synopsys.com*
All Other Questions	**IEEE Computer Society**	*ieeeitc@computer.org*