



# 2020 INTERNATIONAL TEST CONFERENCE

Testing for the Future

NOVEMBER 3 - NOVEMBER 5, 2020

Marriott Washington Wardman Park  
Washington DC, USA

## Call for Papers

International Test Conference is the world's premier venue dedicated to the electronic test of devices, boards and systems—covering the complete cycle from design verification, design-for-test, design-for-manufacturing, silicon debug, manufacturing test, system test, diagnosis, reliability and failure analysis, and back to process and design improvement.

ITC 2020 starts the second half century of the conference. Emerging technologies such as optical, biomedical, and quantum devices will require new test solutions. Artificial Intelligence (AI) and the need for trustworthy devices are providing both new challenges and new opportunities for off-chip and on-chip test. At the same time, more stringent quality requirements, especially in automotive applications, are requiring more efficient test, debug, monitoring, and repair techniques that can transfer to the field.

Authors are invited to submit original, unpublished papers describing recent work in the field of test and design. Of particular interest are works dedicated to the topics listed on the right and/or works related to the conference theme and/or works focused on special tracks such as Automotive, AI, or Security. Authors are also invited to submit practical, industry best practices papers. To make submissions by industrial authors easier, a special short **industrial paper track** that focuses especially on case studies and practical examples has been created. Such papers will be limited to 4 pages in the final proceedings and should not include academic/university authors. Paper submissions for this special track should follow the template posted on the ITC website. Industrial authors who want a longer paper in the proceedings, should submit to one of the regular tracks. Any submissions simultaneously under review or accepted by another conference, symposium or journal, will be summarily rejected.

### Submissions must include:

- Title of paper.
- Name, affiliation, e-mail address of each author.
- The corresponding author(s). ITC will communicate with the corresponding author(s).
- One or two topic(s) from the topic list, or a description of your topic.
- An electronic copy of a complete paper up to **10 pages**, or an extended summary up to **six pages for a normal paper**. Industrial track papers should follow the **posted template**.
- An abstract of 35 words or less to be entered online.

ITC maintains a competitive selection process for technical papers. Submissions must clearly describe the status of the reported work, its contribution, novelty and/or significance. Supporting data, results (priority is often given to papers with results from real designs) and conclusions, and references to prior work must also be included. ITC does not accept submissions that do not meet the specified criteria.

<b>Paper title/abstract due:</b>	<del>March 27, 2020</del>	<b>April 24</b>
<b>Paper final PDF due:</b>	<del>April 3, 2020</del>	<b>May 1</b>
<b>Author notification:</b>	<del>June 15, 2020</del>	<b>June 29</b>
<b>Final manuscript due:</b>	<del>August 14, 2020</del>	<b>August 14</b>

Authors are also invited to submit a **single-page** poster proposal. Posters are a useful way of presenting late-breaking results, getting feedback on an innovative method, or participating without having to write a full paper. Acceptance as a poster does not preclude submission of a more complete work as an ITC paper in 2021. Additional information on poster abstracts and submissions can be found under the author link on the program web site.

<b>Poster submission deadline:</b>	<del>June 22, 2020</del>	<b>July 8</b>
<b>Author notification:</b>	<del>July 20, 2020</del>	<b>August 5</b>

Test Week tutorial and workshop proposals are also welcomed. Deadlines and other information about proposals can be obtained from TTTC at: <http://tab.computer.org/ttcc>

**For detailed information** about the submission process, requirements and deadlines, the selection process and any other questions regarding the program itself or contact information, please consult the ITC web site at <http://www.itctestweek.org>

*ITC invites submissions on the latest advances in test, validation and diagnosis of ICs, boards and systems.*

### Topics of interest include (but not limited to):

3D/2.5D Test  
Adaptive Test in Practice  
Artificial Intelligence (AI)/Machine Learning in Test  
ATE/Probe Card Design  
Automotive Test  
Advances in Boundary Scan  
Bring-Up  
Data Driven Methods  
Data Exchange and Infrastructure  
Defect-oriented Testing  
DFM and Test  
Diagnosis  
Economics of Test  
End-to-End Data Analysis  
End-to-End System Security  
Embedded BIST and DFT  
Emerging Defect Mechanisms  
Field Monitoring, Test, & Debug  
Hardware Security and Trust  
IoT Testing  
Jitter, High-Speed I/O and RF Test  
Known-Good-Die testing  
Memory Test and Repair  
MEMS Testing  
Mixed-Signal and Analog Test  
New Technologies and Test  
On-Chip Test Compression  
Online Test  
Pre-Silicon Verification  
Post-Silicon Validation  
Power Issues in Test  
Protocol-aware Test  
Quantum Device Testing  
Reliability and Resilience  
Scan Based Test  
SoC/SiP/NoC Test  
Silicon Debug  
Simulation and Emulation  
System Test (Applications)  
System Test (Hardware/Software)  
Test-to-Design Feedback  
Test Escape Analysis  
Test Flow Optimizations  
Test Generation and Validation  
Test Resource Partitioning  
Test Standards  
Test Time Analysis and Reduction  
Testing High Speed Optics/Photonics  
Timing Test  
Yield Analysis and Optimization