International Test Conference is the world’s premier venue dedicated to the electronic test of devices, boards and systems—covering the complete cycle from design verification, design-for-test, design-for-manufacturing, silicon debug, manufacturing test, system test, diagnosis, reliability and failure analysis, and back to process and design improvement. At ITC, design, test, and yield professionals can confront challenges faced by the industry, and learn how these challenges are being addressed by the combined efforts of academia, design tool and equipment suppliers, designers, and test engineers.

ITC, the cornerstone of the Test Week™ event, offers a wide variety of technical activities targeted at test and design theoreticians and practitioners, including: formal paper sessions, tutorials, panel sessions, case studies, invited lectures, commercial exhibits and presentations, and a host of ancillary professional meetings.

Authors are invited to submit original, unpublished papers describing recent work in the field of test and design. In addition, authors are invited to submit high quality, practical, industry best practices. Submissions simultaneously under review or accepted by another conference, symposium or journal, will be summarily rejected.

Submissions must include:
- Title of paper.
- Name, affiliation, e-mail address of each author.
- The corresponding author(s). ITC will communicate with the corresponding author(s).
- One or two topic(s) from the topic list, or a description of your topic.
- An electronic copy of a complete paper up to 10 pages, or an extended summary up to 6 pages. Submissions less than 4 pages are rarely accepted.
- An abstract of 35 words or less.

ITC maintains a competitive selection process for papers. Submissions must clearly describe the status of the reported work, its contribution, novelty and significance. Supporting data, results (priority is often given to papers with results from real designs) and conclusions, and references to prior work must also be included. ITC does not accept submissions that do not meet the specified criteria.

| Paper title/abstract due: | February 24, 2017 |
| Paper final PDF due: | March 24, 2017 |
| Author notification: | June 5, 2017 |
| Final manuscript due: | July 24, 2017 |

Authors are also invited to submit a single-page poster proposal. Posters are a useful way of presenting late-breaking results, getting feedback on an innovative method, or participating without having to write a full paper. Acceptance as a poster does not preclude submission of a more complete work as an ITC paper in 2017. Poster proposal abstracts should be no longer than a single page. Additional information on poster abstracts and submissions can be found under the author link on the program web site.

| Poster submission deadline: | June 12, 2017 |
| Author notification: | July 17, 2017 |

Test Week tutorial and workshop proposals are also welcomed. Deadlines and other information about proposals can be obtained from TTTC at: http://tab.computer.org/tttc

For detailed information about the submission process, requirements and deadlines, the selection process and any other questions regarding the program itself or contact information, please consult the ITC web site at http://www.itctestweek.org or email the program chair Peter Maxwell at itctestweek2017@gmail.com.

ITC invites submissions on the latest advances in test, validation and diagnosis of ICs, boards and systems.

**Topics of interest include**
(not limited to):

- 3D/2.5D Test
- Adaptive Test in Practice
- ATE/Probe Card Design
- Advances in Boundary Scan
- Bring-Up
- Data-driven Methods
- Data Exchange and Infrastructure
- Defect-oriented Testing
- DFM and Test
- Diagnosis
- Economics of Test
- End-to-End Data Analysis
- End-to-End System Security
- Embedded BIST and DFT
- Emerging Defect Mechanisms
- Hardware Security and Trust
- IoT Testing
- Jitter, High-Speed I/O and RF Test
- Known-Good-Die testing
- Memory Test and Repair
- MEMS Testing
- Mixed-Signal and Analog Test
- New Technologies and Test
- On-Chip Test Compression
- Online Test
- Pre-Silicon Verification
- Post-Silicon Validation
- Power Issues in Test
- Protocol-aware Test
- Reliability and Resilience
- Scan Based Test
- SoC/SIP/NoC Test
- Silicon Debug
- Simulation and Emulation
- System Test (Applications)
- System Test (Hardware/Software)
- Test-to-Design Feedback
- Test Escape Analysis
- Test Flow Optimizations
- Test Generation and Validation
- Test Resource Partitioning
- Test Standards
- Test Time Analysis and Reduction
- Testing High Speed Optics/Photonics
- Timing Test
- Yield Analysis and Optimization