Call for Papers

November 6-8, 2012
Test Week™: Nov 4 – Nov 9, 2012

Disneyland Hotel
Anaheim, California, USA

International Test Conference is the world's premier venue dedicated to the electronic test of devices, boards and systems—covering the complete cycle from design verification, design- for-test, design-for-manufacturing, silicon debug, manufacturing test, system test, diagnosis, failure analysis and back to process and design improvement. At ITC, design, test, and yield professionals can confront the challenges the industry faces, and learn how these challenges are being addressed by the combined efforts of academia, design tool and equipment suppliers, designers, and test engineers.

ITC, the cornerstone of the Test Week™ event, offers a wide variety of technical activities targeted at test and design theoreticians and practitioners, including: formal paper sessions, tutorials, panel sessions, case studies, a lecture series, commercial exhibits and presentations, and a host of ancillary professional meetings.

Authors are invited to submit original, unpublished papers describing recent work in the field of test and design. In addition, authors are invited to submit practical, industry best practices to be included in application/lecture series sessions. Submissions simultaneously under review or accepted by another conference, symposium or journal, will be summarily rejected.

Submissions must include:

- Title of paper.
- Name, affiliation, mailing address, e-mail address, phone and fax number of each author.
- Designation of the presenter(s). ITC will communicate with the presenter.
- One or two topic(s) from the topic list, or a description of your topic.
- An electronic copy of a complete paper of **6-8 pages (maximum of 10)**, or an extended summary of from three to four pages. **Smaller submissions are rarely accepted.**
- An abstract of 35 words or less.

ITC maintains a competitive selection process for papers. Submissions must clearly describe the status of the reported work, its significance and highlights. Supporting data, results (priority is given to papers with results from real circuits) and conclusions, and references to prior work must also be included. ITC does not accept submissions that do not meet all specified criteria.

Paper submission deadline: March 12, 2012 (Submission deadline is firm.)
Author notification: June 15, 2012
Final manuscript due: August 10, 2012

Authors are also invited to submit a **single-page** poster proposal. Posters are a useful way of presenting late-breaking results, getting feedback on an innovative method, or participating without having to write a full paper. Acceptance as a poster does not preclude submission of a more complete treatment as an ITC paper in 2013. Poster proposal submissions should follow the same guidelines as paper submissions shown above.

Poster submission deadline: June 22, 2012
Author notification: July 16, 2012
One-page paper due: August 3, 2012

Panel organizers are invited to submit panel ideas to highlight new developments and trends in test, to invite group discussion on controversies in test approaches, or to educate the audience on new standards or practices. Submissions must describe the area and possible positions of different panelists. **The deadline for panel proposal submissions is: March 12, 2012**.

Test Week tutorial and workshop proposals are also welcomed. Deadlines and other information about proposals can be obtained from TTTC at: http://tab.computer.org/tttc

For detailed information about the submission process, requirements and deadlines, the selection process and any other questions regarding the program itself or contact information, please consult the ITC web site at http:/www.itctestweek.org.

ITC invites submissions on the latest techniques for the test and diagnosis of ICs, boards and systems.

Conference Focus Topics

Test and DFM
Yield Analysis and Optimization
Embedded BIST & DFT
Reliability Screening
Low-Cost Test
Diagnosis & Silicon Debug
High-Speed I/O and RF Test
Probecard Design
Fault tolerance
System Test
Case Studies
Component-in-System Test

Hot Topics

Adaptive Test
3D Test
Board Test
Defect-based Testing
Industrial Practices
Power Issues in Test
Memory Test and Repair
ATE Hardware and Software
Online Test
Protocol-aware Test
Post-Si Validation
Test Resource Partitioning
Test Flow Optimizations

Regular Topics

Automatic Test Generation
Boundary-Scan
On-Chip Test Compression
Economics of Test
Fault Modeling and Simulation
Online Test
IDDQ and Current Test
Interface Issues
Microprocessor Test
Mixed-Signal and Analog Test
Multisite Test
SiP and KGD Test
Test Standards
Test Quality and Reliability

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