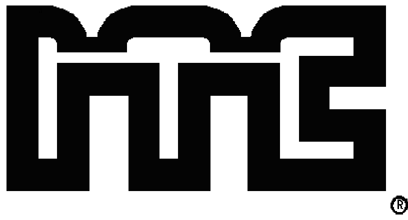

INTERNATIONAL TEST CONFERENCE 2008
Oct. 28 – Oct. 30, 2008
Santa Clara Convention Center
Santa Clara, California, USA

CALL FOR PAPERS

The Cornerstone of Test Week™

Test Week: Oct. 26 – Oct. 31, 2008

International Test Conference is the world's premier conference dedicated to the electronic test of devices, boards and systems—covering the complete cycle from design verification, design-for-test, silicon debug, manufacturing test, diagnosis, failure analysis and back to process and design improvement. At ITC, test and design professionals can confront the challenges the industry faces, and learn how these challenges are being addressed by the combined efforts of academia, design tool and equipment suppliers, designers, and test engineers.

ITC, the cornerstone of the Test Week™ event, offers a wide variety of technical activities targeted at test and design theoreticians and practitioners, including: formal paper sessions, tutorials, panel sessions, case studies, a lecture series, commercial exhibits and presentations, and a host of ancillary professional meetings.

Authors are invited to submit original, unpublished papers describing recent work in the field of test and design. Submissions simultaneously under review or accepted by another conference, symposium or journal, will be rejected. ITC will work cooperatively with others to check for double submissions.

Submissions must include:

- Title of paper.
- Name, affiliation, mailing address, e-mail address, phone and fax number of each author.
- Designation of the presenter(s). ITC will communicate with the presenter.
- One or two topic(s) from the topic list, or a description of your topic.
- An electronic copy of a complete paper of 10 pages maximum, or an extended summary of from four to six pages. **Submissions of less than four pages are rarely accepted.**
- An abstract of 35 words or less.

ITC maintains a highly competitive selection process for papers presented. For details of the selection process, please consult our Web site. Submissions must clearly describe the status of the reported work, its significance and highlights. Supporting data, results and conclusions, and references to prior work must also be included. ITC does not accept submissions that do not meet all specified criteria. Please note that the submission deadline is firm.

Submission Deadline: ***February 15, 2008***
Author Notification: ***May 23, 2008***
Manuscript Deadline: ***July 11, 2008***

Proposals for panels and lecture or application series are also welcome. ***All submissions and presentations must be in electronic format.*** Prospective authors should read the detailed instructions regarding formats and submission requirements that are available on the ITC Web site at***:*** **http://www.itctestweek.org**

Test Week tutorial and workshop proposals are also welcomed. Deadlines and other information about proposals can be obtained from TTTC at: **http://tab.computer.org/tttc**

For further information, check the ITC Web page or contact:

International Test Conference,
Washington, D.C., USA
Tel: +1 202.973.8665 Fax: +1 202.331.0111
E-mail: itc@courtesyassoc.com

Program Chair

Nur Touba, University of Texas at Austin
E-mail: touba@ece.utexas.edu

ITC invites submissions on the latest techniques for testing and diagnosing ICs, boards and systems.

Conference Focus Topics

Adaptive Test
BIST or Embedded Test—Chip and Board
Bring-up Test and Silicon Debug
Design and Test for Reliability
Experiments and Case Studies
High-Speed Digital Test
Low-Cost Test/ATE
On-Chip Test Compression
On-line Test
RF Testing
Test Data Analysis
Test for Nanometer Technologies
Test Resource Partitioning

Hot Topics

Board and System Test
Defect-based Testing
High-Speed I/O Test
Innovative Industrial Test Practice
Power Issues in Test
Test and Design for Manufacturability
Volume Diagnosis and Yield Learning

Regular Topics:

ATE Hardware and Software
ATPG, Test Synthesis
Boundary-Scan
Design-for-Test: Chip, Board and System
Economics of Test
FPGA Test
I_{DDQ} and Current Test
Interface Issues
Loadboard Design and Simulation
MCM and KGD Test
Memory Test
Microprocessor Test
Mixed-Signal and Analog Test
Multisite Test
Production Test Automation
System-on-Chip Test
System-in-Package Test
Test Standards
Test Effectiveness
Wafer Probe