Advance Program

Test Week: November 1 – 6
Conference & Exhibition: November 3 – 5
Austin, Texas USA
On behalf of the over 100 volunteers, International Test Conference (ITC) is proud to present our 40th technical program featuring a full week of test-focused technical activities. The volunteer organizers work tirelessly to bring you a comprehensive program that includes papers, panels, lectures, advanced industrial practices, exhibits, tutorials and workshops on IC test, board test and system test. The 2009 technical program will also include embedded tutorials and a poster session.

Some of the week's highlights include:

**Tutorials:** Test Week™ opens with 12 tutorials covering such diverse topics as high-speed interface testing, design-for-manufacturing, silicon debug and diagnosis, statistical screening, delay test, post silicon validation, failure mechanisms and high-quality test methods for nanometer technologies, analog mixed-signal and RF test, and the economics of test and testability. Leading industry experts provide a wide breadth of knowledge to assist the test engineer in keeping up with new and changing technologies.

**Keynote Address:** The first day of the conference begins with the plenary. Antun Domic, of, Synopsys, will deliver the keynote address, *Design- and Manufacturing-aware Test Is Our Future*.

**Invited Speaker:** The plenary continues with the invited speaker, Shekhar Borkar of Intel. His presentation is titled *Design and Test Challenges for 32 nm and Beyond*.

**Exhibits:** After the plenary session, be sure to visit our dynamic exhibit floor where major industry suppliers will be displaying their latest products and technologies.

**Technical Program:** Our exciting technical program begins after the invited address on Tuesday, and extends for three days and 18 sessions. Find out the latest advances in such hot topics as test compression, power-aware test, and recent advances in delay test, logic diagnosis, silicon debug, and high quality test methods. Learn more about what’s going on in traditional topics such as analog, mixed-signal, RF, microprocessor test and DFT—as well as defects, memory, ATE and board test.

**Lecture Series and Advanced Industrial Practice:** We continue to supplement the program with the lecture series and advanced industrial practice sessions. Lecture Series and Advanced Industrial Practice sessions put a practical perspective on current issues in the test community ranging from volume learning to silicon validation.

**Embedded Tutorials:** This year we will have a separate embedded tutorial track on Wednesday (4 sessions). The embedded tutorials cover testing of 3-D chips, new boundary-scan standards, reliability and test, and jitter fundamentals.

**Posters:** ITC will be continuing its very successful poster session during the “Texas Beer Blast Reception” on Tuesday evening. The poster session provides an opportunity for presenting late-breaking results and getting feedback on innovative methods. It allows for greater interaction between the attendee and presenter.

**IEEE-USA Career Track:** On Thursday there will be a half day career track hosted by IEEE USA. The career track will provide training and guidance for technical professionals looking to improve their career paths.

**Workshops:** Closing out Test Week are three workshops on design for reliability and variability, defect and data driven testing, and test and validation of high-speed analog circuits.

As you can see, Test Week 2009 is packed with numerous opportunities for education and the exploration of exciting new technologies. We encourage you not to miss the industry's leading test conference. You can find more at our Web site [http://itctestweek.org](http://itctestweek.org). We look forward to seeing you in Austin this November.
## Test Week Highlights

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<td>Twelve Full-Day TTTC Tutorials</td>
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<td>A great way to prepare for the ITC Technical program</td>
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<td>Plenary Session - Keynote and Invited Addresses</td>
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<td>Lecture Series and Advanced Industrial Practices</td>
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<td>Special sessions containing introductory and broadening material</td>
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<td>Four Embedded Tutorials</td>
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<td>IEEE-USA Career Track</td>
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<td>World-Class Exhibits</td>
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<td>Corporate Presentations</td>
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<td>The latest technical innovations from our exhibitors and corporate supporters</td>
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<td>Finish your Test Week experience with a choice of three</td>
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<td>Fringe Technical Meetings</td>
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<td>Networking and Social Events</td>
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**Become an ITC corporate supporter**

Take advantage of numerous **advertising and marketing opportunities**

[http://www.itctestweek.org](http://www.itctestweek.org)
### SUNDAY, NOVEMBER 1 – FULL-DAY TUTORIALS

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<th>Time</th>
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<th>Tutorial 2</th>
<th>Tutorial 3</th>
<th>Tutorial 4</th>
<th>Tutorial 5</th>
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</thead>
<tbody>
<tr>
<td>8:30 a.m.</td>
<td>Analyzing, Modeling and Understanding High-Speed Interfaces Using Time Domain Reflectometry</td>
<td>Post-Silicon Validation and Debug</td>
<td>Statistical Screening Methods Targeting “Zero Defect” IC Quality and Reliability</td>
<td>System-in-Package Test Strategies</td>
<td>The Convergence and Interrelationship of Yield, Design for Manufacturability and Test</td>
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<tr>
<td>4:30 p.m.</td>
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### MONDAY, NOVEMBER 2 – FULL-DAY TUTORIALS

<table>
<thead>
<tr>
<th>Time</th>
<th>Tutorial 6</th>
<th>Tutorial 7</th>
<th>Tutorial 8</th>
<th>Tutorial 9</th>
<th>Tutorial 10</th>
<th>Tutorial 11</th>
<th>Tutorial 12</th>
</tr>
</thead>
<tbody>
<tr>
<td>8:30 a.m.</td>
<td>Advanced Topics and Recent Advances in Silicon Debug and Diagnosis</td>
<td>Design for Manufacturability</td>
<td>High-Quality and Low-Cost Delay Testing for VDSM Designs: Challenges and Solutions</td>
<td>Parameter Variations and Self-Calibration/Self-Repair Solutions in Nanometer Technologies</td>
<td>Power-aware Testing and Test Strategies for Low-Power Devices</td>
<td>Practices in Analog, Mixed-Signal and RF Testing</td>
<td>The Economics of Test and Testability</td>
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<td>4:30 p.m.</td>
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### MONDAY, NOVEMBER 2 – SPECIAL PANEL

<table>
<thead>
<tr>
<th>Time</th>
<th>Panel 1</th>
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<tbody>
<tr>
<td>5:00 p.m.</td>
<td>40 Years of Reliable Computing at Stanford CRC</td>
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### MONDAY, NOVEMBER 2 – ITC 40th CONFERENCE YEAR CELEBRATION

<table>
<thead>
<tr>
<th>Time</th>
<th>ITC 40th Conference Reception</th>
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<td>6:30 p.m.</td>
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<td>8:15 p.m.</td>
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### TUESDAY, NOVEMBER 3 – TECHNICAL SESSIONS

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<tr>
<th>Time</th>
<th>Plenary Session</th>
<th>Exibits</th>
<th>Corporate Presentations</th>
<th>Lunch - Complimentary Lunch in Exhibit Hall at Noon</th>
<th>Session 1</th>
<th>Session 2</th>
<th>Session 3</th>
<th>Panel 2</th>
<th>Panel 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>9:00 a.m.</td>
<td>Keynote Address: Design- and Manufacturing-aware Test Is Our Future</td>
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<td>Test Quality and Diagnosis</td>
<td>Boundary-Scan</td>
<td>Poster Preview</td>
<td>Can EDA Help Solve Analog Test and DFT Challenges?</td>
<td>Testing of 3-D Chips: Is There Anything New Under the Sun?</td>
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<tr>
<td>10:30 a.m.</td>
<td>Invited Address: Design and Test Challenges for 32 nm and Beyond</td>
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### TUESDAY, NOVEMBER 3 – POSTER SESSION/Texas Beer Blast Reception

<table>
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<tr>
<th>Time</th>
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<td>7:00 p.m.</td>
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<table>
<thead>
<tr>
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<th>Session 7</th>
<th>Advanced Industrial Practices 2</th>
<th>Embedded Tutorial 1</th>
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<tbody>
<tr>
<td>8:30 a.m. – 10:00 a.m.</td>
<td>RF Testing</td>
<td>Embedded Memory Test and Repair</td>
<td>Industry Roadmap for Adaptive Test</td>
<td>Testing 3-D Chips Containing Through-Silicon Vias</td>
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<table>
<thead>
<tr>
<th>Time</th>
<th>Session 8</th>
<th>Session 9</th>
<th>Session 10</th>
<th>Embedded Tutorial 2</th>
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</thead>
<tbody>
<tr>
<td>8:30 a.m. – 4:00 p.m.</td>
<td>Microprocessor Supply Noise and RF Test</td>
<td>Advances in Test Compression</td>
<td>Limited Access In-Circuit Board Test Techniques</td>
<td>The ABCs of Jitter and How They May Affect You</td>
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<thead>
<tr>
<th>Time</th>
<th>Corporate Presentations</th>
<th>Exhibition</th>
<th>Management Session</th>
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<tr>
<td>9:30 a.m. – 5:30 p.m.</td>
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<td>Free entry 1:00 p.m. – 5:30 p.m.</td>
<td>Decision Making: Trade-Offs and Choices for Testing Today’s Most Complex Chips</td>
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<thead>
<tr>
<th>Time</th>
<th>Session 11</th>
<th>Session 12</th>
<th>Lecture Series 1</th>
<th>Embedded Tutorial 3</th>
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<tr>
<td>10:30 a.m. – 12:00 p.m.</td>
<td>Jitter, Jitter</td>
<td>Test Potpourri</td>
<td>Post-Silicon Test, Debug and Validation</td>
<td>New Boundary-Scan-based Standards</td>
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<thead>
<tr>
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<th>Session 13</th>
<th>Panel 4</th>
<th>Panel 5</th>
<th>Embedded Tutorial 4</th>
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<tr>
<td>12:00 p.m. – 1:30 p.m.</td>
<td>Test Techniques for ADC/Mixed Signal Devices</td>
<td>Power Faults – What Is Our Tolerance for Defects?</td>
<td>Physically-aware DFT: Is It Worth All the Heavy Lifting?</td>
<td>Reliability and Test over the Product Life Cycle</td>
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<thead>
<tr>
<th>Time</th>
<th>Panel 6</th>
<th>Panel 7</th>
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<tbody>
<tr>
<td>1:30 p.m. – 3:30 p.m.</td>
<td>Predictive Solutions for Test—The Next DFT Paradigm?</td>
<td>How (Un)Affordable Is the True Cost of Test?</td>
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### THURSDAY, NOVEMBER 5 – TECHNICAL SESSIONS

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<th>Session 16</th>
<th>Lecture Series 2</th>
<th>Lecture Series 3</th>
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<td>8:00 a.m. – 12:00 p.m.</td>
<td>Improving Yield on Your Same Old ATE</td>
<td>Getting Working Silicon</td>
<td>Verification and Diagnostic ATPG</td>
<td>Elevator Talks</td>
<td>Innovative Approaches to Performance Test</td>
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<table>
<thead>
<tr>
<th>Time</th>
<th>Exhibits</th>
<th>Advanced Industrial Practices 3</th>
<th>Panel 7</th>
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<tbody>
<tr>
<td>9:30 a.m. – 2:00 p.m.</td>
<td>Free entry 9:30 a.m. – 2:00 p.m.</td>
<td>Test for Yield</td>
<td>How (Un)Affordable Is the True Cost of Test?</td>
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<thead>
<tr>
<th>Time</th>
<th>Session 17</th>
<th>Session 18</th>
<th>Lecture Series 3</th>
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<tr>
<td>10:30 a.m. – 12:00 p.m.</td>
<td>X Handling for MISR Signatures</td>
<td>Innovative Solutions</td>
<td>Innovative Approaches to Performance Test</td>
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<table>
<thead>
<tr>
<th>Time</th>
<th>Panel 6</th>
<th>Panel 7</th>
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<tbody>
<tr>
<td>12:00 p.m. – 1:30 p.m.</td>
<td>Predictive Solutions for Test—The Next DFT Paradigm?</td>
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### THURSDAY, NOVEMBER 5 – WORKSHOPS

<table>
<thead>
<tr>
<th>Time</th>
<th>Test and Validation High-Speed Analog Ckts.</th>
<th>Design for Reliability and Variability</th>
<th>Defect- and Data-driven Testing</th>
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<tr>
<td>4:00 p.m. – 6:30 p.m.</td>
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<th>Time</th>
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### FRIDAY, NOVEMBER 6 – WORKSHOPS

<table>
<thead>
<tr>
<th>Time</th>
<th>Test and Validation High-Speed Analog Ckts.</th>
<th>Design for Reliability and Variability</th>
<th>Defect- and Data-driven Testing</th>
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<tr>
<td>8:00 a.m. – 4:00 p.m.</td>
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TTTC TEST TECHNOLOGY EDUCATION PROGRAM (TTEP) 2009

The Tutorials & Education Group of the IEEE Computer Society Test Technology Technical Council (TTTC) organizes a comprehensive set of Test Technology Tutorials to be held in conjunction with several TTTC-sponsored technical meetings worldwide. The mission of the Test Technology Educational Program (TTEP) is to serve test and design professionals by offering fundamental education and expert knowledge in state-of-the-art test technology topics. TTEP offers tutorial participants the opportunity to earn official certification from IEEE Computer Society TTTC. Each full-day tutorial corresponds to four TTEP units. Upon completion of sixteen TTEP units, official recognition in the form of an IEEE TTTC Test Technology Certificate will be presented to the participant. For further information regarding TTEP, please visit http://tab.computer.org/ttc/ttcg/ttep/

At ITC09, TTTC/TTEP is pleased to present twelve full-day tutorials on topics of current interest to test professionals and researchers. All tutorials qualify for credit towards IEEE TTTC certification under the TTEP program. Five tutorials are held on Sunday, November 1st, and seven on Monday, November 2nd. Each tutorial requires a separate registration fee (see ITC registration form or www.itctestweek.org for further information). Admission for on-site registrants is subject to availability.

Tutorail attendees receive study material, breakfast, lunch, and coffee breaks. The study material includes a hardcopy of the presentation and bibliographical material. Tutorial registration, coffee and pastry are available at 7:00 a.m. on Sunday and Monday.

Sunday  8:30 a.m. – 4:30 p.m.  more Sunday tutorials >

TUTORIAL 1
Analyzing, Modeling and Understanding High-Speed Interfaces Using Time Domain Reflectometry

Presenter W. Maichen

Description Keeping theory and mathematics to a minimum, this presentation aims to develop an intuitive understanding of high-speed transmission line behavior. This is an important topic for anyone concerned with design, analysis, troubleshooting, or qualification of high-speed interconnects like backplanes, printed circuit boards, high-speed serial links, cables, connectors, sockets etc. Using a compact time domain reflectometer (TDR) we will perform a variety of life, real-time demonstrations (free-hand experiments) to investigate topics like delay and characteristic impedance, reflections, impedance mismatches, parasites, lumped and distributed crosstalk, differential signaling, and others. We will show how to extract quantitative data for transmission lines and parasites and use them to build equivalent models to be used in transmission path simulation. Towards the end we will compare TDR with the traditionally more common analysis based on network analyzers and show strengths and weaknesses in either approach.

TUTORIAL 2
Post-Silicon Validation and Debug

Presenters N. Nicoli, B. Vermeulen, J. Stinson

Description Pre-silicon verification methods work with models of the design and are therefore limited by the inherent trade-off between accuracy and runtime. Designs are sent to fabrication when the confidence level is high enough; unfortunately, functional and electrical design bugs can still remain undetected and slip through to prototype silicon. Errors that slip through require fixing as soon as possible once detected on the prototype. Hence, the pre-silicon verification transitions to post-silicon validation and debug upon return of first silicon samples from the fab. The continued need for more effective and efficient debugging methods and instruments is expected to drive innovative new debug research over the forthcoming years. In this tutorial, we present the basic concepts and the recent advances in this area.

TUTORIAL 3
Statistical Screening Methods Targeting “Zero Defect” IC Quality and Reliability

Presenter A. Singh

Description Integrated circuits have traditionally all been tested identically in the manufacturing flow. However, as the detection of subtle manufacturing flaws becomes ever more challenging and expensive in aggressively scaled nanometer technologies, innovative new statistical screening methods are being developed that attempt to improve test effectiveness and optimize test costs by adaptively subjecting “suspect” parts to more extensive testing. The idea is similar to security screening at airports. Such methods fall into two broad categories: those that exploit the statistics of defect distribution on wafers, and those that exploit the correlation in the variation of process and performance parameters on wafers. This tutorial presents test methodologies that span both these categories, and illustrates their effectiveness with results from a number of recently published experimental studies on real production circuits by key manufacturers.
TUTORIAL 4
System-in-Package Test Strategies
Presenter Y. Zorian

Description Today’s miniaturization and performance requirements result in the usage of high-density advanced packaging technologies, such as system-in-package (SIP), direct-chip-attach, chip-scale packaging (CSP), and ball-grid arrays (BGA). Due to their physical access limitation, the complexity and cost associated with their test and diagnosis are considered major issues facing their use. This tutorial provides comprehensive knowledge of test solutions for advanced packages by placing particular emphasis on: test and debug approaches for bare dies; testing schemes for flip-chips used in direct-chip-attach, CSP and SIP packages; testing bare substrates, and finally, test, diagnosis and repair techniques for assembled modules.

TUTORIAL 5
The Convergence and Inter-relationship of Yield, Design for Manufacturability and Test
Presenters S. Venkataraman, R. Aitken

Description The tutorial goal is to show how design for yield (DFY) and design for manufacturability (DFM) are tightly coupled into what we conventionally think of as test. As process geometries shrink, the line between defects and process variation blurs to the point where it is essentially nonexistent. As feature sizes reduced to 90 nm and below, systematic mechanism-limited yield loss began to appear as a substantial component in yield loss due to the interaction between design and manufacturing. The basics of yield and what fabs do to improve defectivity and manage yield are described. DFM techniques to analyze the design content, flag areas of design that could limit yield, and make changes to improve yield are discussed. In DFM/DFY circles, it is common to speak of defect limited yield, but it is less common to think of test limited yield, yet this concept is common in DFT (e.g. IDDQ testing, delay testing). Test techniques to close the loop by crafting test patterns to expose the defect-prone feature and circuit marginality through ATPG, and by analyzing silicon failures through diagnosis to determine the features that are actually causing yield loss and their relative impact are covered. This tutorial will provide background needed for DFT practitioners to understand DFY and DFM, and see how their work relates to it. The ultimate goal is to spur attendees to conducting their own research in the area, and to apply these concepts in their jobs.

Discount Rates!
Register by October 12
TUTORIAL 6  Cancelled
Advanced Topics and Recent Advances in Silicon Debug and Diagnosis

Presenters S. Venkataraman, M. Abramovici, R. Aitken

Description The increasing design complexity along with the emergence of new failure mechanisms in the nanometer regime has significantly increased the complexity of verification, validation and manufacturing ramp of ICs. When pre-silicon verification and validation uncovers design bugs, the process of diagnosing and debugging these issues is called design error diagnosis. From the time a new chip comes back from the fab until high-volume production can start, the chip goes through functional silicon validation and debug to make sure it is free of design errors, and defect diagnosis and failure analysis to solve yield problems. These activities, referred to as silicon debug and diagnosis, have become the most time-consuming phase in the development cycle of a new design, increasing to about 33% of the total time. This is a consequence of the increasing design complexity, along with the emergence of new failure mechanisms in nanometer technologies. Long time-to-volume and low manufacturing yield have a greatly detrimental impact on the economic viability and the overall success of a product. This tutorial covers the state of the art and the full spectrum of topics in silicon validation and debug and defect diagnosis ranging from the basic concepts to advanced applications and new DFD techniques. We will also describe successful debug and diagnosis methods used in real industrial products, industrial experiences, and case studies. Finally we will discuss future directions and challenges.

TUTORIAL 7 Cancelled
Design for Manufacturability

Presenters Y. Zorian, J.-A. Carballo

Description In addition to designing the functionality, today’s SOC necessitates designing for manufacturability, yield and reliability. Such requirements are fundamentally transforming the current SOC design methodology. Techniques for enhancing manufacturability, yield, and reliability, or “DFX”, include yield enhancement techniques, resolution enhancement techniques, new or restricted design rules, variability-aware design, and the addition of a special family of embedded IP blocks, called Infrastructure IP blocks. The latter blocks are meant to ensure manufacturability of the SOC and to achieve adequate levels of yield and reliability. The infrastructure IP leverages the manufacturing knowledge and feeds back the information into the design phase. This tutorial analyzes the key trends and challenges resulting in manufacturing susceptibility and field reliability that necessitate the use of the above DFX techniques. Then, it concentrates on several examples of each of these techniques.

TUTORIAL 8 Cancelled
High-Quality and Low-Cost Delay Testing for VDSM Designs: Challenges and Solutions

Presenters M. Tehranipoor, K. Chakrabarty, J. Rearick

Description As technology scales to 32 nm and functional frequency and density continue to rise, many factors and parameters have shown significant impact on design and test of chips. Test engineers must now deal with many new challenges such as IR-drop and power supply noise (PSN) effects on chip performance, signal integrity and crosstalk effects on path delay, high test pattern volume, low fault/defect coverage, small-delay defect test pattern generation and fault simulation, process variation effects, high cost of test implementation and application, and unmodeled faults. This tutorial provides practice-oriented solutions to the above challenges. The tutorial is designed to provide design and test engineers with in-depth knowledge on high-quality delay test generation for reduced escape and increased in-field reliability.

TUTORIAL 9
Parameter Variations and Self-Calibration/Self-Repair Solutions in Nanometer Technologies

Presenters S. Mukhopadhyay, R. Rao, P. Elakkumanan, S. Bhunia

Description Device level parameter variations caused by process imperfections, environmental variations (e.g., temperature) and aging effects (e.g., NBTI, HCI) manifest as variations in delay, leakage and noise margin in logic and memory circuits leading to manufacturing yield loss and reliability degradation. In this tutorial, we focus on post-silicon on-chip self-calibration and self-repair schemes for logic and memory circuits that can improve parametric yield and reliability. This tutorial will discuss causes of parametric variations and aging effects; present efficient techniques for on-chip and on-line sensing and characterization of manufacturing variations and aging effects in device and circuit parameters; discuss circuit and system level techniques for self-calibration and self-repair of logic and memory circuits; and explore self-repairing systems for mixed-signal design. The audience will be introduced to the post-silicon strategies for self-calibration and self-repair that constitutes a promising class of solutions to address variation induced parametric failures and associated test challenges.
Monday 8:30 a.m. – 4:30 p.m.

TUTORIAL 10
Power-aware Testing and Test Strategies for Low-Power Devices
Presenters P. Girard, N. Nicoli, X. Wen

Description Power dissipation is becoming a critical parameter during manufacturing test as the device can consume much more power during test than during functional mode of operation. In the meantime, elaborate power management strategies, like voltage scaling, clock gating or power gating techniques, are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test, and power-aware test is therefore increasingly becoming a major consideration during design-for-test and test preparation for low power devices. This tutorial provides knowledge in this area. It is organized into three main parts. The first one gives necessary background and discusses issues arising from excessive power dissipation during test application. The second part provides comprehensive knowledge of structural and algorithmic solutions that can be used to alleviate such problems. The last part surveys low power design techniques and shows how these low power devices can be tested safely without affecting yield and reliability.

TUTORIAL 11
Practices in Analog, Mixed-Signal and RF Testing
Presenters S. Abdennadher, S. Shaikh

Description The objective of this tutorial is to present existing industry ATE solutions and alternative solutions to ATE testing for mixed-signal and RF SOCs. These techniques greatly rely upon DFT and BIST structures. The tutorial presents the basic concepts in analog and RF measurements (eye diagram, jitter, gain, power compression, harmonics, noise figure, phase noise, BER, etc.). Several industrial examples of production testing of mixed-signal and RF devices, such as, SERDES transceivers, PHYs, HSIO, and RF transceivers are also presented. The block-DFT solutions are presented for PLLs, CDR, equalizers, filters, mixers, AGC, LNAs, DACs and ADCs. The testing of high-speed IO interfaces, such as, PCIe, and SATA, etc., and the new design trends in RF systems such as MIMO- and SIP-based systems and their testability are also presented.

TUTORIAL 12
The Economics of Test and Testability
Presenters S. Davidson, H. Colby, L. Ungar

Description Test economics provides a way of quantifying the costs and benefits of test, and helps a test engineer choose an effective test strategy. Classical microeconomics is far more sophisticated than what is found in test economics papers. Recent work in behavioral economics, known to the public through bestsellers such as “Freakonomics,” has shown that classical assumptions about the behavior of economic actors are wrong. This tutorial will summarize existing work in test economics, provide background on microeconomic and behavioral economics concepts that are of interest to test and DFT engineers, and will show their applicability to test. The student will emerge with the ability to do traditional cost and benefit modeling, and with a deeper understanding of the economic principles that affect the cost and benefits of test. The researcher will emerge with the tools to make a much better case for the benefits of the proposed research.
Four embedded tutorials form a track, running all day Wednesday, giving ITC attendees the chance to get up-to-speed on exciting new test technologies. These tutorials are presented free-of-charge to all registered ITC conference attendees.

8:30 a.m.–10:00 a.m.

EMBEDDED TUTORIAL 1
Testing 3-D Chips Containing Through-Silicon Vias

Presenters E. J. Marinissen, IMEC; Y. Zorian, Virage Logic

This tutorial provides an overview of manufacturing through-silicon via (TSV)-based 3-D chips and the test challenges associated with. It also demonstrates the necessary flows for wafer-level and module-level test, and the infrastructure IP needed to perform embedded test, diagnosis and redundancy/repair for 3-D chips.

10:30 a.m.–12:00 p.m.

EMBEDDED TUTORIAL 2
The ABCs of Jitter and How They May Affect You

Presenters M. Li, Altera; B. Achkir, Cisco Systems; A. Meixner, T. Schumacher, Intel

This tutorial will focus on the fundamentals of jitter: the types of jitter, what causes jitter, how jitter is measured and the effects of jitter. In addition, current "test case" examples will be provided to demonstrate the impact of jitter on newer, high-speed technologies.

1:30 p.m.–3:30 p.m.

EMBEDDED TUTORIAL 3
New Boundary-Scan-based Standards

E 3.1 Doing More with Less—An IEEE 1149.7 Standard for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture

Presenter A. Ley, ASSET InterTech

IEEE Std 1149.7 offers a means to reduce chip pins dedicated to test (and debug) access while enhancing the functionality of the test access port (TAP) as a complementary superset of the original IEEE Std 1149.1 (JTAG). This tutorial will provide a comprehensive overview of what 1149.7 is, how it is implemented and the benefits provided by the standard.

E 3.2 IEEE P1687 (IJTAG) Hardware and Software Architectures

Presenters A. Crouch, ASSET InterTech; J. Rearick, AMD

IEEE P1687 specifies a description language for embedded instruments which are accessible via boundary-scan. This embedded tutorial will focus on the hardware infrastructure required to support the proposed standard, how that infrastructure can be used to access embedded instruments and how that access path can be described. In addition, the proposed standard also describes how to "program" the instrument to implement desired features associated with that instrument.

4:00 p.m.–5:30 p.m.

EMBEDDED TUTORIAL 4
Reliability and Test over the Product Life Cycle

Presenters J. Carulli, Texas Instruments; S. Mitra, Stanford University; A. Haggag, Freescale Semiconductor

This tutorial will begin by discussing the basics of reliability and what they mean to the test engineer, and will then explore EFR/parametric shift/HTOL and what they mean to the test engineer. Finally, the tutorial will conclude with a discussion on "resilient circuits adapting to reliability mechanism and what they mean to the test engineer.
Exhibits opening: Tuesday 10:30 a.m. – 6:30 p.m.
Wednesday 9:30 a.m. – 5:30 p.m., Thursday 9:30 a.m. – 2:00 p.m.

FREE EXHIBITS-ONLY ADMISSION

ITC is offering free exhibits-only registration to visit the exhibit hall on Wednesday from 1:00 p.m. to 5:30 p.m. and on Thursday from 9:30 a.m. to 2:00 p.m. On-site registration for this special opportunity begins on Wednesday at 1:00 p.m. at the ITC registration area in the Austin Convention Center.

Visit the international exhibition that includes the latest high-technology test, design and service products.
Participating Exhibitors*

Aehr Test Systems
Aries Electronics, Inc.
ASSET InterTech, Inc.
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Pickering Electronics Ltd.
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Test Insight
Test Spectrum, Inc.
Tokyo Electron Limited (TEL)
TSSI – Test Systems Strategies, Inc.
Unitechno USA, Inc.
Verigy
Virage Logic
XJTAG

* As of publication date.
As the vanguards of the semiconductor industry approach the 32-nanometer node and start planning the jump to the 22-nanometer node, a number of fundamental challenges are emerging, which force a thorough rethinking of the role of test.

Over the last 10 years, we have stretched the limits of scaling beyond the imaginable. We are using 193-nanometer lithography—the same lithography that we had introduced at 90 nanometers!—to draw 32-nanometer gates, with a maximum allowable error of 2 nanometers. We are dealing with approximately 100 atoms of dopant elements, which we are trying to spread uniformly across the surface—and the thickness!—of a gate channel which is less than 3-nanometer—i.e., 10 atoms—thick.

As a result, the number of microbridges, especially resistive bridges, is increasing with immersion lithography. The impact of nonuniformity on timing and power variability at the 32-nanometer node is in the 50% range, and increasing. The number of small-delay and transition-delay defects does increase on average by 3X from one technology node to the next. The overall number of test patterns vs. stuck-at-fault ones is 5X at 65 nanometers and will skyrocket to 30X at 32 nanometers. Test compression above the 100-200X is very design dependent, is complex and costly, and cannot cope with the test data volume increase due to the nanometer manufacturing and design for low power requirements.

Like drugs have often counter-indications and side effects, even nanometer design and manufacturing are not immune of drawbacks, which require that test assume an equal station, is accounted for by them, and inter-operates thoroughly with them. Both implementation and yield management tools may feed test with the design- and manufacturing-related information it needs to keep the problem manageable, while guaranteeing the desired quality and cost of results.

In this keynote, Dr. Domic will describe how design, manufacturing, and test can join forces, and collaborate to battle the nanometer challenges.

About the speaker: Dr. Antun Domic joined Synopsys in April of 1997. In his current position, Dr. Domic manages the Implementation Group, responsible for Synopsys’ flagship synthesis and physical design solutions, test automation, signal integrity, power analysis and timing and formal verification products.

Before joining Synopsys, Dr. Domic spent several years at Cadence Design Systems, where he was engineering vice president for the place and route, synthesis and timing areas. Previously, he worked in the microprocessor group of Digital Equipment Corporation in Hudson, Massachusetts, where he managed the development of CAD tools for synthesis and automatic layout used to design several generations of Alpha and VAX microprocessors. Prior to joining Digital, he worked at MIT Lincoln Laboratories and Honeywell Information Systems.

Through the years, Dr. Domic has been involved in the organization of several technical conferences, including the Design Automation Conference (DAC), Design Automation & Test Europe (DATE), the International Conference on Computer-Aided Design (ICCAD), and the International Conference on Computer Design (ICCD). He participates frequently in industry panels regarding design and manufacturing technologies.

Dr. Domic holds a B.S. in mathematics and electrical engineering from the University of Chile in Santiago, Chile, and a Ph.D. in mathematics from the Massachusetts Institute of Technology in Cambridge, Massachusetts.
Comput performance increased by orders of magnitude in the last few decades, made possible by continued technology scaling, improving transistor performance to increase frequency, increasing integration capacity to realize novel architectures, and reducing energy consumed per logic operation to keep power dissipation within limit. The technology treadmill will continue to fulfill the performance demand; however, it’s the same physics that helped you in the past that will now pose some barriers—“Business as usual” will not be an option.

Billions of transistors of integration capacity will be available to enable novel designs. These complex chips will have to be designed with emphasis on the system design, optimized at the system level, and with new design methodologies rather than today’s custom or application-specific chip design methodologies.

Testing should not be an after-thought. Design for test and manufacturing methodology will not be sufficient, and test hardware will have to become part of the design itself. Abundance of transistors, but with gradual faults like variations, intermittent faults like soft-errors, and slowly varying faults caused by aging will demand system resiliency. Testing such complex systems with the aid of resiliency will open doors to entirely new paradigms, and testing will have entirely new meaning.

This talk will discuss challenges and potential solutions in all disciplines, such as architecture, system design, circuits & layout, resiliency, and testing to realize these novel systems.

About the speaker: Shekhar Borkar graduated with a M.Sc. in Physics from University of Bombay, MSEE from University of Notre Dame in 1981, and joined Intel Corporation. He is an Intel Fellow, director of Microprocessor Research, and an IEEE Fellow. His research interests are high-performance and low-power digital circuits, and high-speed signaling.
1:30 p.m. – 3:30 p.m.

SESSION 1
Test Quality and Diagnosis
S. Biswas, NVIDIA (Chair)

1.1 Comparing the Effectiveness of Deterministic Bridge Fault and Multiple-Detect Stuck Fault Patterns for Physical Bridge Defects: A Simulation and Silicon Study
S. K. Goel, N. Devta-Prasanna, M. Ward, LSI

1.2 Defect-oriented Cell-aware ATPG and Fault Simulation for Industrial Cell Libraries and Designs

1.3 Test Effectiveness Evaluation Through Analysis of Readily Available Tester Data
Y.-T. Lin, S. Blanton, Carnegie Mellon University

1.4 Application of Nonparametric Statistics of the Parametric Response for Defect Diagnosis
R. Gudavalli, R. Daasch, Portland State University; P. Nigh, D. Heaberlin, IBM

SESSION 2
Boundary-Scan
J. Johnson, SiliconAid Solutions (Chair)

2.1 Testing Bridges to Nowhere—Combining Boundary-Scan and Capacitive Sensing
S. Sunter, Mentor Graphics; K. Parker, Agilent Technologies

2.2 3rd-Generation Intel IBIST: The Full Vision Realized
J. Nejedlo, R. Khanna, D. Ellis, Intel

2.3 Fast Extended Test Access via JTAG and FPGAs
S. Devadze, I. Aleksejev, Testonica Lab; A. Jutman, R. Ubar, Tallinn University of Technology

2.4 Boundary-Scan Adoption—An Industry Snapshot with Emphasis on the Semiconductor Industry
P. Geiger, Dell; S. Baekovich, Cisco Systems

SESSION 3
Poster Preview
W. Eklow, Cisco Systems (Chair)

4:00 p.m. – 5:30 p.m.

SESSION 4
Delay Test and Power-aware Test
M. Tehranipoor, University of Connecticut (Chair)

4.1 Minimizing Outlier Delay Test Cost in the Presence of Systematic Variability
D. Drmanac, B. Bolin, L.-C. Wang, University of California, Santa Barbara; M. Abadir, Freescale Semiconductor

4.2 Accurate Measurement of Small Delay Defect Coverage of Test Patterns
N. Devta-Prasanna, S. K. Goel, A. Gunda, M. Ward, P. Krishnamurthy, LSI

4.3 Capture Power Reduction Using Clock-Gating-aware Test Generation
K. Chakravadhanula, V. Chickenmane, B. Keller, P. Gallagher, P. Narang, Cadence Design Systems

SESSION 5
Understanding Frequency Behavior on a Device
A. Crouch, ASSET InterTech (Chair)

5.1 AutoRex: An Automated Post-Silicon Clock Tuning Tool
D. Tadesse, R. Bahar, Brown University; J. Grodstein, Intel

5.2 Using Transition Test to Understand Timing Behavior of Logic Circuits on UltraSPARC™ T2
L.-C. Chen, P. Dickinson, P. Dahlgren, S. Davidson, O. Caty, K. Wu, Sun Microsystems

5.3 Data Learning Techniques and Methodology for Functional Fmax Prediction
L. Wang, J. Chen, P.-H. Chang, University of California, Santa Barbara; J. Zeng, S. Yu, M. Mateja, AMD
8:30 a.m. – 10:00 a.m.

SESSION 6
RF Testing
K. Schaub, Advantest America (Chair)

6.1 Built-in EVM Measurement for OFDM Transceivers Using All-Digital DFT
E. Yilmaz, A. Nassery, S. Ozev, Arizona State University; E. Acar, Duke University

6.2 Enabling GSM/GPRS/EDGE EVM Testing on Low-Cost Multisite Testers
B. Lai, C. Rivera, K. Waheed, Texas Instruments

6.3 Accurate Low-Cost AM/AM and AM/PM Measurement Using Distortion-to-Amplitude Conversion
S. Sen, S. Devarakond, A. Chatterjee, Georgia Institute of Technology

SESSION 7
Embedded Memory Test and Repair
Y. Zorian, Virage Logic (Chair)

7.1 Fault Diagnosis for Embedded Read-only Memories
J. Tyszer, Poznan University of Technology; N. Mukherjee, A. Pogiel, J. Rajski, Mentor Graphics

7.2 A Novel Test Flow for One-time-Programming Applications of NROM Technology
C-Y. Chin, C-M. Chang, M. Chao, National Chiao Tung University; Y-T. Tsou, Macronix International

7.3 A Comprehensive TCAM Test Scheme: An Optimized Test Algorithm Considering Physical Layout and Combining Scan Test with At-Speed BIST Design
H-H. Wu, University of Maryland; J-N. Lee, M-C. Chiang, P-W. Liu, C-F. Wu, Realtek Semiconductor

10:00 a.m. – 12:00 p.m.

SESSION 8
Microprocessor Supply Noise and I/O Test
T. Wood, AMD (Chair)

F. Stellari, P. Song, IBM T.J. Watson Research Center; J. Sylvestri, D. Miles, O. Forlenza, D. Forlenza, IBM

8.2 Voltage Transient Detection and Induction for Debug and Test
R. Petersen, P. Pant, P. Lopez, A. Barton, J. Ignowski, D. Josephson, Intel

8.3 Cache-resident Self-Testing for I/O Circuity
S. Gurusamy, D. Bertanetti, P. Jakobsen, J. Rearick, AMD

SESSION 9
Advances in Test Compression
B. Keller, Cadence Design Systems (Chair)

9.1 Compression-aware Pseudo-Functional Testing
F. Yuan, Q. Xu, The Chinese University of Hong Kong

9.2 Compression Based on Deterministic Vector Clustering of Incompatible Test Cubes
J. Tyszer, D. Czos, Poznań University of Technology; G. Mrugalski, N. Mukherjee, J. Rajski, Mentor Graphics

9.3 On Simultaneous Shift- and Capture-Power Reduction in Linear Decompressor-based Test Compression Environment
X. Liu, Q. Xu, The Chinese University of Hong Kong

10:00 a.m. – 12:00 p.m.

SESSION 10
Limited Access In-Circuit Board Test Techniques
J. Grelish, Intel (Chair)

10.1 An Economical, Precise and Limited-Access In-Circuit Test Method for Pulse-Width Modulation (PWM) Circuits
A. Yeh, J. Chou, M. Lin, Test Research

10.2 Augmenting Board Test Coverage with New Intel Powered-Opens Boundary-Scan Instruction
C-L. Tee, T-H. Tan, C-C. Ng, Intel

10.3 An Outlier Detection-based Approach for PCB Testing
X. He, A. Jayasumana, Y. Malaiya, Colorado State University; K. Parker, S. Hird, Agilent Technologies

conference year
1:30 p.m. – 3:30 p.m.

SESSION 11
Jitter, Jitter, Jitter!
T. Munns, Munns Consulting (Chair)

11.1 SSC-applied Serial ATA Signal Generation and Analysis by Analog Tester Resources
H. Okawara, Verigy

11.2 A Robust Method for Identifying a Deterministic Jitter Model in a Total Jitter Distribution
T. Yamaguchi, K. Ichiyama, M. Ishida, Advantest Laboratories; H. Hou, Advantest America

11.3 Dynamic Arbitrary Jitter Injection Method for >6.5-Gb/s SerDes Testing

11.4 A Timestamping Method Using Reduced-Cost ADC Hardware
T. Lyons, Teradyne

SESSION 12
Test Potpourri
J. Bedsole, Freescale Semiconductor (Chair)

12.1 Novel Architecture for On-Chip Path Delay Measurement
X. Wang, M. Tehranipoor, University of Connecticut; R. Datta, Texas Instruments

12.2 Low-Cost Test Point Insertion Without Using Extra Registers for High-Performance Design
H. Ren, M. Kusko, V. Kravets, R. Yaari, IBM

12.3 Test Economics for Homogeneous Manycore Systems
L. Huang, Q. Xu, The Chinese University of Hong Kong

12.4 Physical Defect Modeling for Fault Insertion in System Reliability Test
Z. Zhang, K. Chakrabarty, Duke University; Z. Wang, X. Gu, Cisco Systems

4:00 p.m. – 5:30 p.m.

SESSION 13
Test Techniques for ADCs/Mixed-Signal Devices
M. Abadir, Freescale Semiconductor (Chair)

13.1 BIST Scheme for RF VCOs Allowing the Self-Correction of the CUT
L. Testa, H. Lapuyade, Y. Desai, O. Mazouffre, J. Beguere, IMS Laboratory; J. Carbonero, STMicroelectronics

13.2 A2DTest: A Complete Integrated Solution for On-Chip ADC Self-Test and Analysis
B. Mallane, V. O’Brien, C. MacNamee, T. Fleischmann, University of Limerick

13.3 New Modeling Methods for Bounded Gaussian Jitter (BGJ)/Noise (BGN) and Their Application in Jitter/Noise Estimation Testing
M. Shimanoouch, M. Li, D. Chow, Altera

4:00 p.m. – 6:00 p.m.

MANAGEMENT SESSION
Decision Making Trade-Offs and Choices for Testing Today’s Most Complex Chips
Y. Zorian, Virage Logic (Chair)

M 1 Manufacturing Test Challenges of Very-Low-Cost and High-Performance SOCs
R. Galivanchc, Intel

M 2 Striking the Balance Between Production Test Cost, Quality and Yield
K. Arabi, Qualcomm

M 3 Managing DFX for Highly Complex SOCs
A. Majumdar, AMD

M 4 Testing of High-Yield, Low-Cost, Programmable Systems-on-Chip
K. Chakrabarty, Cypress Semiconductor
8:30 a.m. – 10:00 a.m.

SESSON 14
Improving Yield on Your Same Old ATE
B. Parnas (Chair)

14.1 Thermal Characterization of BIST, Scan Design and Sequential Test Methodologies
M. Simsir, N. Jha, Princeton University

14.2 Cost-effective Approach to Improve EMI Yield Loss
H-C. Ko, D-Y. Chang, King Yuan Electronics;
C-N. Hu, Oriental Institute of Technology

14.3 A Development Platform and Electronic Modules for Automated Test Up to 20 Gbps
D. Keezer, C. Gray, A. Majid, Georgia Institute of Technology; D. Minier, P. Ducharme, IBM Canada

SESSION 15
Getting Working Silicon
C. Schuermeyer, Mentor Graphics (Chair)

15.1 Microprocessor System Failures Debug and Fault Isolation Methodology
E. Amyeen, S. Venkataraman, M-W. Mak, Intel

15.2 Design for Failure Analysis Inserting Replacement-type Observation Points for LVP
J. Nonaka, T. Ishiyama, K. Shigeta, NEC

15.3 Feature-based Similarity Search with Application to Speedpath Analysis
N. Callegari, L-C. Wang, University of California, Santa Barbara; P. Bastani, Intel

10:30 a.m. – 12:00 p.m.

SESSON 16
Verification and Diagnostic ATPG
J. Dworak, Brown University (Chair)

16.1 Speeding-Up Bounded Sequential Equivalence Checking with Cross-Timeframe State-Pair Constraints from Data Learning
C-L. Chang, H-P. Wen, National Chiao Tung University; J. Bhadra, Freescale Semiconductor

16.2 An Ant Colony Optimization Technique for Abstracted-guided State Justification
M. Li, M. Hsiao, Virginia Tech

16.3 Diagnostic Test Generation for Transition Faults Using a Stuck-at ATPG Tool
2:00 p.m. – 3:30 p.m.

SESSION 17
X-Handling for MISR Signature
T. Rinderknecht, Mentor Graphics (Chair)

17.1 X-Alignment Techniques for Improving the Observability of Response Compactors
O. Sinanoglu, S. Almukhaizim, Kuwait University

17.2 Industrial Case Study for X-Canceling MISR
J-S. Yang, N. Touba, The University of Texas at Austin; S-Y. Yang, T.M. Mak, Intel

17.3 Test Point Insertion Using Functional Flip-Flops to Drive Control Points
J-S. Yang, N. Touba, The University of Texas at Austin; B. Nadeau-Dostie, Mentor Graphics

SESSION 18
Innovative Solutions
V. Mehta, NVIDIA (Chair)

18.1 Running Scan Test on Three Pins: Yes We Can!
J. Moreau, P. Armagnat, T. Droniou, P. Lebourg, STMicroelectronics

18.2 A Novel Array-based Test Methodology for Local Process Variation Monitoring
T-C. Luo, M. Wu, K-T. Li, C-C. Hsia, H-C. Tseng, C-I. Huang, Y-Y. Chang, S. Pan, K-L. Young, TSMC; M. Chao, National Chiao Tung University

18.3 Fast Circuit Topology-based Method to Configure the Scan Chains in Illinois Scan Architecture
S. Donglikar, M. Banga, M. Chandrasekar, M. Hsiao, Virginia Tech

Free Exhibits Admission
Wednesday 1:00 p.m.–5:30 p.m.
Thursday 9:30 a.m.–2:00 p.m.
ITC's Lecture Series provides a showcase for topics that are important to the test industry either because they are at the leading edge of technology or because they are foundational in nature. All three sessions will provide a solid background for as well as a snapshot of the current state of the art.

Advanced Industrial Practices (AIP) sessions provide an opportunity for attendees to learn the latest methods and techniques used by industry leaders in addressing some of today's most important test challenges. This year's AIP sessions include interesting presentations from the Southwest Test Workshop, which focuses on wafer- and die-level testing, a session on how test can be used for yield improvement, and a session on the critical problem of validating an IC after the first silicon comes back from the fab.
The corporate track allows you to stay on top of the latest commercial products in the semiconductor test industry and helps you understand how the innovations behind the products can add value to your employer. Whereas the technical program allows you to gain an in-depth understanding of the latest technical innovations, the corporate track allows you to actually gain an in-depth understanding of how some of the technology innovations impact the product portfolios of companies. In this interactive forum, executives of ITC exhibitors or sponsors will present their latest products and sometimes product roadmaps. Moreover, company representatives are free to hand out relevant literature such as papers or marketing material. Typical presentations include case studies, best practices, and testimonials. The corporate presentation schedule will be distributed at the conference.
Tuesday 5:30 p.m. – 7:00 p.m.

The poster session will be held in conjunction with the Texas Beer Blast Reception. Poster previews will be given in Session 3 on Tuesday at 1:30 p.m.

W. Eklow, Cisco Systems (Chair/Coordinator)

PO 1 Eliminating Product Infant Mortality Failures Using Prognostic Analysis
L. Losik, Failure Analysis

PO 2 Automatic Diagnostic Tool for Analog Mixed-Signal and RF Load Boards
S. Kannan, B. Kim, University of Alabama, Tuscaloosa; G. Srinivasan, F. Tuczzer, R. Antley, Texas Instruments

PO 3 Scalyable and Efficient Integrated Test Architecture
M. Portolan, S. Goyal, Bell Labs Ireland; B. Van Treuren, Alcatel-Lucent Bell Labs

PO 4 Very-Low-Voltage Testing of Amorphous Silicon TFT
J. Li, S-T. Shen, W-H. Liu, I-C. Cheng, National Taiwan University

PO 5 Low-Power Multichains Encoding Scheme for SOC in Low-Cost Environment
J-C. Rau, P-H. Wu, Tamkang University

PO 6 Power- and Thermal-constrained SOC Test Scheduling
C. Yao, K. Saluja, P. Ramanathan, University of Wisconsin-Madison

PO 7 Power Scan: DFT for Power Switches in VLSI Designs
B-C. Bai, C-M. Li, National Taiwan University; A. Ki[il], E. Tsai, K-C. Wu, Faraday Technology

PO 8 IEEE P1687 I/JTAG: A Presentation of Current Technology
K. Posse, Avago Technologies; A. Crouch, ASSET InterTech; J. Rearick, Advanced Micro Devices

PO 9 Test Mode Entry and Exit Methods for IEEE P1581-compliant Devices
H. Ehrenberg, GOEPEL Electronics

PO 10 A Novel Multisite Testing Technique by Using Frequency Synthesizer
B. Kim, I-C. Park, G. Song, W. Choi, B-Y. Kim, K. Lee, C-Y. Choi, Samsung Electronics

PO 11 Design-for-Secure-Test for Crypto Cores
Y. Shi, N. Togawa, M. Yanagisawa, T. Ohitsuki, Waseda University

PO 12 Noninvasive RF Built-in Testing Using On-chip Temperature Sensors
J. Altet, D. Mateo, E. Aldrete, Universitat Politecnica de Catalunya; M. Onabajo, J. Silva-Martinez, Texas A&M University

PO 13 NAND Flash Testing: A Preliminary Study on Actual Defects
A. Virazel, P-D. Mauroux, A. Bosio, L. Dilillo, P. Girard, S. Pravossoudovich, LIRMM; B. Godard, ATMEL

PO 14 Built-in Self-Test for Error Vector Magnitude Measurement of RF Transceiver
B. El Kassir, C. Kelma, NXP Semiconductors; B. Jarry, M. Campovecchio, XILIM

PO 15 Fine-Resolution Double-Edge Clipping with Calibration Technique for Built-in, At-Speed Delay Testing
C-H. Cheng, C-I. Chung, S-W. Chang, Feng-Chia University

PO 16 Portable Simulation/Emulation Stimulus on an Industrial-Strength SOC
M. Bose, F. Torres, R. Srinivasta, J. Ruiz, J. Bhdr, Freescale Semiconductor; H-P. Wen, Chiao Tung University

PO 17 Test Infrastructures Evaluation at Transaction Level
N. Hatami, S. Di Carlo, P. Prinetto, Politecnico di Torino

PO 18 Trace Signal Selection for Debugging Electrical Errors in Post-Silicon Validation
Q. Xu, X. Liu, The Chinese University of Hong Kong

PO 19 Defect Coverage of Nonintrusive Board Tests (NBT): What Does It Mean When a Nonintrusive Board Test Passes?
A. Ley, ASSET InterTech

PO 20 What is IEEE P1149.8.1 and Why?
K. Parker, Agilent Technologies; J. Burgess, Intel

PO 21 Manufacturing Data: Maximizing Value Using Component-to-System Analysis
M. Kann, Cisco Systems

PO 22 High-Speed I/O Test Cable Assembly Interfaces for Next-Generation Multi-Gigabit Serial Protocols
J. Vana, A. Barr, R. Scherer, A. Joshi, 3M
All IEEE-USA Career Track events are on Thursday, November 5

The IEEE-USA career track provides conference attendees with three sessions focused on helping engineers expand their career prospects. Whether it's starting a consulting practice, becoming an entrepreneur or if it's becoming an innovator in your current position, this track provides information and insight that can lead you to an independent future.

Entrance to the career track sessions is free for all paid ITC Test Week registrants. Check the "I will attend" line on the registration form. Your career track entrance ticket will be issued to you when you pick up your badge at the Austin Convention center.

7:30 a.m. – 8:00 a.m.
Continental Breakfast

8:00 a.m. – 9:30 a.m.
Innovating Your Career—What It Takes to Step Yourself Ahead of the Competition

Peggy Hutcheson, CEO, The Odyssey Group, Inc.

Innovation is the new business buzz word. CEOs, venture capitalists and politicians are looking to inject innovative concepts into their business to improve productive and create new products. Electrical, computer science and telecommunications engineers will play a significant role in developing new strategies to improve business. Come to this IEEE-USA sponsored workshop to learn about how to identify your innovative potential and how you can apply that in your current work environment.

9:30 a.m. – 11.00 a.m.
Entrepreneurship and Financing: What You Need to Know Panel Discussion: Angels, VCs and Entrepreneurs (to be invited)

Mauro Togneri (Moderator), IEEE-USA Committee Chair for Entrepreneurs Activities

Many of us have at one point in time believed that we could do a certain task better than the current business model being applied by top firms. What stopped you from taking on the big boys in business—financing, motivation and life circumstance? Come hear entrepreneurs share their experience and wisdom about the pros and cons of starting their own business. “Venture Capitalists” will also be on hand to give you insight on why some entrepreneurial efforts get financing and others don’t.

11:00 a.m. – 12.00 p.m.
Becoming a Consultant: The Nuts and Bolts

Gary Blank IEEE-USA Member-at-Large and Chair, IEEE Alliance of Consultants Networks

If you are concerned about possibly losing your job in this slowing economic climate and considering making a rapid transition from full-time corporate position to being a full-time independent consultant then this session is for you. This session will provide 1. An Introduction to modern consulting and the consulting marketplace. 2. A discussion of the reasons to become a consultant and how these reasons influence your success as a consultant. 3. The details necessary to start your business and expand it rapidly.

About the speaker: Dr. Peggy Hutcheson is known for her expertise in connecting employees to changing work roles. She helps individuals develop individual career management skills and works with organizations to build career processes that ensure a workforce that is continually developing and contributing in important ways. She is president of The Odyssey Group, Inc., a consulting firm with offices in Atlanta, Georgia, and Washington, D.C. She is a long term member and former Chair of IEEEUSA’s Employment and Career Services Committee and serves on the Steering Committee of the Innovation Institute. She can be reached at p_hutcheson@odysseygroupinc.com.

About the speaker: Mauro has been in industrial instrumentation and control industries since 1961 as an engineer, independent consultant, owner, manager, vice president, president, and outside director, designed products and systems, founded and managed the growth of entrepreneurial technology based companies with worldwide operations. He is currently a management consultant after retiring in December 2003. Mauro holds a number US patents in the instrumentation field and is the cofounder and cochair of the IEEE-USA Entrepreneurial Activities Committee and the Entrepreneurs Village virtual community in 2005. He is assisting the PACE Committee with web community development. Mauro is also a member of the IEEE-USA Innovation Institute Steering Committee and the past chair and current member of the Intellectual Property Committee of USAB/IEEE USA since 1988.

About the speaker: Gary Blank received a BS degree in 1959 from Illinois Institute of Technology, a MS degree in 1960 from the University of Idaho, and a Ph.D. degree in 1963 from the University of Wisconsin. All degrees are in electrical engineering. He was a principal staff engineer at Honeywell, Litton Guidance and Control Systems, and Teledyne Systems. He was a full-time professor of electrical engineering at Illinois Institute of Technology, Northern Illinois University, Marquette University; and part time at U.C.L.A. and the University of Florida. He has been a successful self-employed consultant in industry for 35 years to over 30 client companies and the U.S. Navy. He has published many technical papers. He is the IEEE-USA senior member-at-large and a life senior member of IEEE.
Monday, 5:00 p.m. – 6:30 p.m.

Panel 1  40 Years of Reliable Computing at Stanford CRC

B. Bottoms, 3MTS (Moderator) • N. Touba, The University of Texas at Austin, S. Mitra, Stanford University (Organizers)

This panel will celebrate contributions to reliable computing over the past 40 years by the Stanford Center for Reliable Computing (CRC) under the leadership of Professor Edward J. McCluskey.

Panelists: J. Abraham, University of Texas • H. Hao, Samsung • J. Li, National Taiwan University • D. Lu, Intel • S. Mitra, Stanford University • P. Nigh, IBM • N. Saxena, NVIDIA • P. Shirvani, NVIDIA • N. Touba, University Texas at Austin

Tuesday, 4:00 p.m. – 5:30 p.m.

Panel 2  Can EDA Help Solve Analog Test and DFT Challenges?

C. Moore, Maxim Integrated Products (Moderator) • R. Datta, Texas Instruments and S. Sunter, Mentor Graphics (Organizers)

This panel will explore whether and where the EDA industry could improve DFT and testing of analog functions.

Panelists: K. Arabi, Qualcomm • C. Force Texas Instruments • S. Sunter, Mentor Graphics • N. Nandra, Synopsys • S. Taneja, Cadence Design Systems

Panel 3  Testing of 3-D Chips: Is There Anything New Under the Sun?

K. Chakrabarty, Duke (Moderator) • E.J. Marinissen, IMEC and S. K. Goel (Organizers)

3-D chips based on through-silicon vias are hot in the design and processing community. What new test challenges do they bring forward, and how much of the learnings from MCM and SIP testing can be applied in this field?

Panelists: P. Franzon, North Carolina State University • M. Laisne, Qualcomm • E.J. Marinissen, IMEC • K. Parker, Agilent Technologies • Y. Zorian, Virage Logic

Wednesday, 4:00 p.m. – 5:30 p.m.

Panel 4  Power Faults—What is Our Tolerance for Defects?

J. Rearick, AMD (Moderator) • G. Giles, AMD (Organizer)

Modern ICs have power saving features that are actuated by logic but may or may not be observed in logic. How much power savings loss does a defect in the circuitry of such a power saving feature have to cause for us to regard the chip as defective?

Panelists: J. Bedsole, Freescale Semiconductor • M. Bienek, AMD • V. Chickermane, Cadence Design Systems • H. Mair, Texas Instruments • H. Yeager, Intel

Panel 5  Physically Aware DFT: Is It Worth All the Heavy Lifting?

K. Butler, Texas Instruments (Moderator) • L. Winemberg, Freescale Semiconductor (Organizer)

Physically aware DFT tools exist today. However, they often require very long run times and result in very large patterns sets. Are these new tools really necessary or are the old tried-and-true stuck-at and transition fault models all that we need?

Panelists: N. Ahmed, Texas Instruments • R. Aitken, ARM • M. Tehranipoor, University of Connecticut • D. Walker, Texas A&M

Thursday, 2:00 p.m. – 3:30 p.m.

Panel 6  Predictive Solutions for Test—The Next DFT Paradigm?

R. Aitken, ARM (Moderator) • C. Allsup, Synopsys (Organizer)

Some designers have suggested the traditional approach to implementing test is outdated; instead, “predictive solutions” are needed to make architectural tradeoffs and predict test outcomes before implementation. Our panel will discuss the feasibility of predictive solutions, what design and test tradeoffs they should consider, and how accurate they should be.

Panelists: K. Arabi, Qualcomm • S. Bhatia, Atrenta • J. Rearick, AMD

Panel 7  How (Un)Affordable Is the True Cost of Test?

S. Davidson, Sun Microsystems (Moderator) • R. Parekhji, Texas Instruments (India) (Organizer)

Test cost means different things to different teams in terms of spending as well as affordability. Panelists from design, EDA, fab and system companies will debate on: (1) What is the incurred cost? (2) What is necessary? (3) What is affordable?

Panelists: J. Caralli, Texas Instruments • A. Crouch, ASSET InterTech • S. Davidson, Sun Microsystems • B. Eklow, Cisco Systems • S. Slupsky, GSA
IEEE Computer Society Test Technology Technical Council Workshops

Thursday and Friday

General Workshop Information
Three workshops are being held in parallel immediately following ITC 2009 at the Austin Convention Center. They start with an opening address on Thursday afternoon, November 5, followed by a technical session. A reception for all workshop participants will be held on Thursday evening. The remaining the technical sessions will be held on Friday, November 6. The technical scope of each workshop is described below.

Workshop Registration
All workshop participants require registration. To register in advance for one of the workshops, do so online or by faxing the download form. Otherwise, register on-site at regular rates during Test Week at the ITC registration counter at the Austin Convention Center. Admission for on-site registrants is subject to availability. Discount workshop registration rates apply until October 12, 2009. Workshop registration includes the opening address, technical sessions, digest of papers, workshop reception, break refreshments, continental breakfast and lunch. See Registration for further details.

Digest of Papers
A digest of papers will be distributed only to attendees at the workshops as informal proceedings.

Workshop Schedule
All three workshops will adhere to the same schedule:

<table>
<thead>
<tr>
<th>Thursday, November 5</th>
<th>Friday, November 6</th>
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<tbody>
<tr>
<td>Registration</td>
<td>Registration</td>
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<tr>
<td>2:00 p.m. – 7:00 p.m.</td>
<td>7:30 a.m. – 10:00 a.m.</td>
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<tr>
<td>Opening Address</td>
<td>Technical Sessions</td>
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<tr>
<td>4:00 p.m. – 4:30 p.m.</td>
<td>8:00 a.m. – 4:00 p.m.</td>
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<td>Technical Session</td>
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<tr>
<td>Reception</td>
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<td>7:00 p.m. – 9:00 p.m.</td>
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Note: Workshop schedule is subject to change

Further Information
For more information on the three workshops contact their organizers by e-mail or check the TTTC Web site http://computer.org/tttc
TVHSAC: IEEE International Workshop Test and Validation of High-Speed Analog Circuits

**Scope:** In this workshop, we will examine various issues associated with test and validation of high-speed analog circuits, including innovative solutions for high parametric coverage and lower test cost. In IC designs today, analog content is no longer a small portion of silicon as it was in the past. With various interfaces such as PCIe, DDR, Display-IO, HT, and other components such as PLLs, DACs, Temperature Sensors, the proportion of silicon die area covered by analog circuits is continually increasing with each design generation. Starting with 65-nm process technology, a growing market need for high speeds, large bandwidths and small geometries have made designs a lot more complex in terms of testability and manufacturability. Majority of test for analog portions of a chip have been marginalized to characterization on the ATE and boards. This characterization is often planned around various electrical and thermal corners and the outcome is heavily dependent on process technology. More often than not, rigorous testing of the full range of properties of an analog circuit is neglected during production-ramp and production. Prime among the many reasons for this lack of rigor in of analog circuits test is overall test cost. Representative topics include, but are not limited to the following:

- Analog DFT and test methods
- Characterization of analog cores
- Analog IP design and verification issues
- Fault models, defect modeling
- ATE for high-speed analog measurement
- On-die high-speed sensors and test structures

General Chair: A. Majumdar, Amitava.Majumdar@amd.com
Program Chair: V. Ganti, ganti@apple.com

DRV: 2nd IEEE International Workshop on Design for Reliability and Variability

**Scope:** As silicon-based CMOS technologies are fast approaching their ultimate limits reliability is threatened by issues such as process, voltage and temperature variability, accelerated aging and wear-out, radiation-induced soft-errors and crosstalk. These problems are creating barriers to further technology scaling and are forcing the introduction of new process and design solutions aimed at maintaining acceptable levels of reliability. As elimination of these issues is becoming increasingly difficult, various design techniques including self-calibration and fault tolerance are emerging as the most promising design approaches to circumvent them. However, these techniques may incur significant area, power or performance penalties. Thus, to enable their adoption by industrial teams, there is need for new solutions which minimize these penalties, together with automation tools. The goal of this workshop is to create an informal forum to discuss those design, EDA and test innovations enabling chips to maintain acceptable reliability levels at reasonable cost. Topics to include:

- Reliability issues in advanced CMOS
- Variability-aware design
- Radiation effects in advanced CMOS
- Design-for-reliability
- Fault-tolerant architectures
- Variability mitigation
- Self-calibrating architectures
- Online monitoring of circuit parameters
- Design automation for fault tolerance
- Design automation for fault tolerance
- Variability-insensitive architectures
- Reliability assessment tools

General Chairs: Y. Zorian, zorian@viragelogic.com, M. Nicolaidis, Michael.nicolaidis@imag.fr

D3T: IEEE Workshop on Defect- and Data-driven Testing

**Scope:** New test-data-based methodologies are required to detect, monitor, and comprehend the various defect mechanisms at sub-50-nm technology nodes. Data-driven testing (DDT) has been in practice for a number of years. It is now gaining attention more than ever in adaptive test. DDT can provide feedbacks on which tests to add/remove, or test subsets (e.g., reduced MINVDD test sets.) It can also be utilized for improving quality of logic test patterns (e.g., small delay defect, defect-based) vs. outlier analysis tests (e.g., MINVDD, \(I_{DDQ}\)). However, test data has not been easily accessible by smaller companies and researchers in academia. These issues will be discussed in this year’s D3T workshop. The D3T is aimed at addressing these and other issues. Paper presentations on topics related to the workshop’s theme and those given below are expected to generate active discussion on the challenges that must be met to ensure high IC quality through the end of the decade.

- Outlier identification
- Data-driven testing
- Test data analysis
- Adaptive testing
- Data mining methods for test data processing
- Low-voltage testing
- Noise and crosstalk testing
- Nanometer test challenges
- Defect coverage and Metrics
- Mixed-current/voltage testing
- Economics of defect-based testing
- Fault localization and diagnosis

General Chair: M. Tehranipoor, tehrami@engr.uconn.edu
Program Chair: A. Crouch, acrouch@asset-intertech.com
Fringe Technical Meetings

Sunday to Thursday

ITC arranges for meeting space for appropriate IEEE- or Computer Society TTTC-sponsored groups wishing to hold their meetings during Test Week, November 1 – November 5.

Sunday, November 1
9:00 a.m. – 6:00 p.m. VTS PC Meeting – off site  C. Thibeault & M. Renovell Claude.Thibeault@etsmtl.ca

9:00 a.m. – 5:00 p.m.  IEEE P1687 Working Group (IJTAG)  K. Posse ken.posse@avagotech.com

Tuesday, November 3
10:30 a.m. – 11:30 a.m. IEEE P1687 Working Group (IJTAG)  K. Posse ken.posse@avagotech.com
11:30 a.m. – 1:00 p.m. IEEE D&T Editorial Board*  T. Cheng timcheng@ece.ucsb.edu
1:00 p.m. – 2:00 p.m. TTTC ExCom  A. Singh singhad@auburn.edu
2:00 p.m. – 3:00 p.m. TTTC Senior Leadership Council  Y. Zorian zorian@viragelogic.com
3:00 p.m. – 4:00 p.m. TTTC Tutorial & Education Group  D. Gizopoulos dgizop@unipi.gr
4:00 p.m. – 5:00 p.m. TTTC Communications Group  C. Metra Cecilia.Metra@unibo.it

Wednesday, November 4
9:00 a.m. – 10:00 a.m. TTTC TMRC*  C-H. Chiang chenhuan@alcatel-lucent.com
10:00 a.m. – 11:00 a.m. TTTC Standing Committee Group*  M. Nicolaidis michael.nicolaidis@imag.fr
11:00 a.m. – 12:00 p.m. TTTC Standards Group (TTSG)  R. Kapur rkapur@synopsys.com
12:00 p.m. – 2:00 p.m. ETS Steering Committee  H-J. Wunderlich wu@informatik.uni-stuttgart.de
2:00 p.m. – 4:00 p.m. TTTC Operation Committee*  A. Singh singhad@auburn.edu
4:00 p.m. – 5:00 p.m. IEEE P1581 Working Group  H. Ehrenberg h.ehrenberg@goepelusa.com

Thursday, November 5
8:00 a.m. – 10:00 a.m. IEEE 1149.6 Working Group  W. Eklow beklow@cisco.com
10:00 a.m. – 12:00 p.m. IEEE 1149.1 Working Group  C.J. Clark cclark@INTELLITECH.COM
2:00 p.m. – 5:00 p.m. IEEE 1149.8.1 Working Group  J. Burgess jeff.burgess@intel.com

*Members or Invitation Only
ITC 40th Conference Year Celebration

Monday, November 2, 6:30 p.m. – 8:15 p.m.
Hilton Austin   Salon C – Forth Floor

All registered ITC attendees and registered exhibitors are cordially invited to join us for beverages and light fare. Come and meet your colleagues at this special social event. Renew your contacts and build your professional network by making valuable new connections.

Continue your debates and examine the poster presentations at the complimentary beer and snack event that follows the panels.

Texas Beer Blast
Hilton Austin
Salon H – Sixth Floor
Tuesday, November 3
5:30 – 7:00 p.m.

WORKSHOP RECEPTION
Hilton Austin – Room 406
Thursday, November 5
7:00 – 9:00 p.m.
All Test Week activities require a registration badge for admittance. Register in advance online or by faxing the download form. Otherwise, register on-site at regular rates during Test Week at the ITC registration counter at the Austin Convention Center. See page 26 for registration hours. To obtain a substantial discount on ITC Full-Conference Registration, Tutorial Registration and Workshop Registration, register no later than October 12, 2009.

**ITC Full-Conference Registration** includes ITC technical paper and panel sessions, lecture and advance industrial application series, exhibits, ITC welcome reception, break refreshments, ITC proceedings CD-ROM and ITC tote and mug. Registration **does not include** the tutorials on Sunday and Monday or the workshops on Thursday and Friday. May purchase additional CD-ROM proceedings at $25 each; one presentation CD-ROM at $25.

Special on-site ITC registrations: One-Day; Three-Day Exhibits-only and Free Wednesday afternoon and Thursday Exhibits-only, are available only at the ITC registration counter at the Santa Clara Convention Center.

**ITC One-Day Registration** includes ITC technical program activities, exhibits and refreshments for the day of registration only, and ITC proceedings CD-ROM and ITC tote and mug. May purchase: additional CD-ROM proceedings at $25; one presentation CD-ROM at $25.

**ITC Three-Day Exhibits-only Registration** includes the exhibits and lunches on Tuesday and Wednesday.

### Registration Fees

<table>
<thead>
<tr>
<th>Discount Rates*</th>
<th>Full Conference</th>
<th>1-Day-only Conference</th>
<th>3-Day Exhibits-only</th>
<th>One Tutorial</th>
<th>Workshop</th>
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<td>IEEE/CS Member</td>
<td>$495</td>
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<td>IEEE/CS Student Member</td>
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<tr>
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*not available after October 12, 2009

### Refunds

Registration fees paid by October 12 are refundable on written request to ITC, c/o BADGEGuys, 1959 Jester Circle, Lawrenceville, GA 30043 USA, postmarked or faxed (+1 678.669.1802) by October 12, 2009. A $75 processing fee is charged for each refund.
### Conference and Tutorials

<table>
<thead>
<tr>
<th>Day</th>
<th>Time</th>
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<tbody>
<tr>
<td>Sat, Oct 31</td>
<td>7:30 a.m. – 5:00 p.m.</td>
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<tr>
<td>Sun, Nov 1</td>
<td>7:30 a.m. – 7:00 p.m.</td>
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<tr>
<td>Mon, Nov 2</td>
<td>7:30 a.m. – 5:00 p.m.</td>
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<tr>
<td>Tues, Nov 3</td>
<td>7:30 a.m. – 5:00 p.m.</td>
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<td>Wed, Nov 4</td>
<td>7:30 a.m. – 5:00 p.m.</td>
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<tr>
<td>Thurs, Nov 5</td>
<td>7:30 a.m. – 1:30 p.m.</td>
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<tr>
<td>Fri, Nov 6</td>
<td>2:00 p.m. – 7:00 p.m.</td>
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### Workshops

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### Exhibitors

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<tbody>
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<tr>
<td>7:30 a.m. – 5:00 p.m.</td>
</tr>
</tbody>
</table>

### Need More Registration Information?

Contact the ITC office  
2025 M Street, NW, Suite 800, Washington, DC 20036, USA  
Tel. +1 202.973.8665 Fax. +1 202.331.0111
ITC Proceedings Distribution

All ITC full-conference and one-day attendees, including students, will receive free of charge at the conference the ITC proceedings on CD-ROM.

Ordering Additional Proceedings During Advance Registration
Full-conference attendees may also order additional copies of the CD-ROM proceedings, beyond the free copy, at $25 each.

Purchasing Additional Proceedings at the Conference
Additional copies of the CD-ROM proceedings may be purchased on-site for $25 each.

A valuable option!

ITC Technical Paper Presentation CD-ROM

The ITC Program Committee has compiled the slides used for this year’s paper presentations and placed them in a CD-ROM*. You can review sessions that you attended and cover those that you could not attend. They will only be available at the conference to registered full- and one-day conference attendees, including students—one per person. The cost for this very popular item is only $25 each. The CDs may be ordered with your advance registration or purchased on-site.

The paper presentation slides make the perfect complement to the full manuscripts in the proceedings, as they contain the latest data.

*Some authors have chosen not to participate. These papers will be indicated in a list provided on the CD box. Slides used in panel sessions and corporate presentations are not included.
Reserve a hotel room online. For further housing information, send e-mail to jay@connectionshousing.com or call 1.800.262.9974 or 404.842.0000. Fax 404.601.7441.

1. Reservations are now being accepted. Assignments will be made in the order of request.
2. Reservations may be made online or by fax using the downloaded housing form.
3. All room must be guaranteed with a major credit card.
4. Reservations will be confirmed within three to five business days after the day that the reservation was made. If you have faxed your form and do not hear from us within seven days, please contact Jay Pierce at 1.800.262.9974 or 404.842.0000.
5. Cancellation: Guests must cancel their reservation more than 72 hours prior to arrival (three full days prior to the scheduled date of arrival). Cancellations may be subject to a penalty fee equal to one night’s room rate and tax if less than 72 hours notice is given.
6. If requesting double accommodations, please provide the name of the second guest and specify one or two beds.
7. Please verify the arrival and departure dates on the confirmation letter sent from Connections. The departure date is the day that you leave the hotel—not the last night of your stay.
8. Check-in time is 3:00 p.m. For any early arrival to be guaranteed, the room must be booked for the previous night.
9. Deadline date for housing submissions is October 15, 2009. After October 15, rooms at the ITC rate are subject to availability.
10. All reservation requests must be made through Connections, not with the individual hotels.
11. Changes and cancellations must be submitted in writing via e-mail to Jay Pierce.

### Hotel Rates (exclusive of taxes)

**Hilton Austin**
- (1 to 2 guests) $179
- (3 guests) $199
- (4 guests) $219

**Courtyard by Marriott Austin – Downtown**
- (1 to 4 guests) $169

**Residence Inn by Marriott Austin – Downtown**
- (1 to 4 guests) $169

**Hampton Inn Austin – Downtown**
- (1 guest) $169
- (2 to 4 guests) $179

**Four Seasons Austin – Downtown**
- (1 to 2 guests) $199

**Radisson Hotel Austin – Town Lake**
- (1 to 2 guests) $155
- (3 guests) $165
- (4 guests) $175
Location

The ITC conference and all associated Test Week events will be held at the Austin Convention Center, Austin, Texas. Austin is the capital of the state of Texas, and its 1888 capitol building is an interesting landmark. Also of interest are the main campus of The University of Texas and the Lyndon B. Johnson Library and Museum. Close to the convention center is the lively East Sixth Street entertainment district which features many restaurants and a variety of music in the “Live Music Capital of the World”. The downtown area has miles of waterfront trails suitable for walking and jogging and is also home to the largest urban bat population in the US whose spectacular flight can be observed just before sunset. For more information about Austin, visit http://www.austintexas.org. Lodging for Test Week is in several hotels in the vicinity of the convention center.

Travel

Air

Austin-Bergstrom International Airport (AUS) offers nonstop flights to both U.S. and international cities. The airport offers easy access and is located only 7.5 miles from downtown Austin. Information can be found at http://www.ci.austin.tx.us/austinairport Taxi fare from the airport to downtown area hotels is approximately $23. Two shuttles connecting to conference hotels are:

**Super Shuttle – 512-258-3826 or 800-258-3826**

Fare is $13 one-way per person from the airport to the downtown hotels. Group service is also available for $54 per van for up to 7 people. Upon arrival at the airport, check in at the Super Shuttle ticket counter located near baggage claim on the lower level of the airport. No reservation is necessary. Vans are assigned on a first come first served basis, and service is available 24 hours a day. http://www.supershuttle.com

**Capital Metro’s Airport Flyer – Route #100**

This limited-stop transit service provides an economical fare of 50 cents each way between the airport and the downtown area. Inbound service stops at 6th and Congress streets in proximity to the downtown area hotels. Outbound service to the airport has a pick-up stop at 7th and Congress streets. **Weekday** inbound service to downtown begins at 5:20 a.m. through 11:20 p.m. and weekday outbound service to the airport begins at 5:00 a.m. through 10:57 p.m. **Saturday** inbound service to downtown begins at 6:40 a.m. through 10:40 p.m. and Saturday outbound service to the airport begins at 6:17 a.m. through 10:18 p.m. **Sunday** inbound service to downtown begins at 8:00 a.m. through 10:40 p.m. and Sunday outbound service to the airport begins at 7:37 a.m. through 10:18 p.m. http://www.capmetro.org

Car

The Austin Convention Center has two parking garages: at 2nd Street and Brazos (two blocks West) and at 5th Street and Red River (Northeast corner). The fee is $7.00/day.

**Route from Austin Bergstrom International Airport**

The Austin Convention Center is about 11 miles from the Austin Bergstrom International Airport. Take Bastrop Hwy TX-71 W (TX-71 becomes E. Ben White Blvd) for 5.6 miles. Turn slight right onto S I-35 (.2 miles). Merge onto I-35 N / US-290 E / US-81N (2.8 miles). Take Exit 234B toward 2nd-4th Streets / 1st Street / Cesar Chavez (.1 miles). Stay straight to go onto I-35 N (.1 miles). Turn left onto E. 1st Street / Cesar Chavez Street E (.2 miles). Facility is on your right.
1. The Advance Program was created with Adobe Acrobat 8.0 on 21-October-2009.

2. Best viewed at least 75%.

3. The program will be updated periodically as new material is available—check back often.

4. Navigate using the tabs at the top of each page.

5. Use underlined links in the At-a-Glance to find specific items.

6. Most of the papers have a “key feature.” Place your cursor over the shaded paper number to see it.

   

6. For more information contact:

   

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